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Design and simulation of a single-stage amplifier using MOSFET transistor

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Abstract
Signal amplification is an indispensable step in electronic circuits because it is impractical to use direct signals from sensors to control devices without an amplifier circuit. Some input signals are very small and need amplification to be large enough to affect the circuit and control devices. In this paper, we continuously present the steps to design a single-stage Common Source (CS) amplifier using a voltage-divider biased MOSFET transistor [1-6]. After analyzing and calculating the DC and AC operation modes of the amplifier circuit, we proceed to simulate it on Multisim software to verify the theoretical results. The example in this article can also serve as reference materials for electrical and electronics students in technical universities.
Keywords: *amplifier, audio frequency amplification, bias, MOSFET transistor, Multisim.*

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I. INTRODUCTION

Amplification is a controlled energy conversion process, where the energy of a DC power supply (which does not contain information) is converted into AC energy (with transformation rules that carry the required information). In other words, this is an analog signal processing process. The article provides basic knowledge of a voltage amplifier, analysis of a single-stage CS amplifier circuit using MOSFET transistor connected in a voltage divider configuration. We then take an example to illustrate the steps to design an audio frequency amplifier circuit with some given parameters.

II. THEORETICAL BASIS

2.1. General Introduction to Amplification

An amplifier is used to convert relatively "weak" signals, i.e., in the range of microvolts (μV) or millivolts (mV) and with low energy, into signals with larger amplitude [1-6]

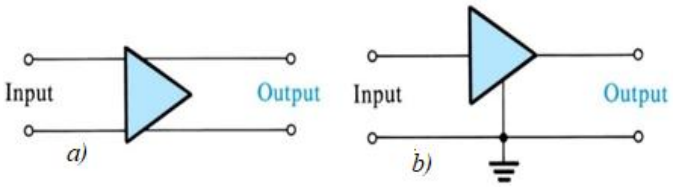


Figure 1: *(a) Schematic symbol of an amplifier circuit; (b) Amplifier with a common point (ground) between the input and output ports.*

2.2 Voltage Amplifier

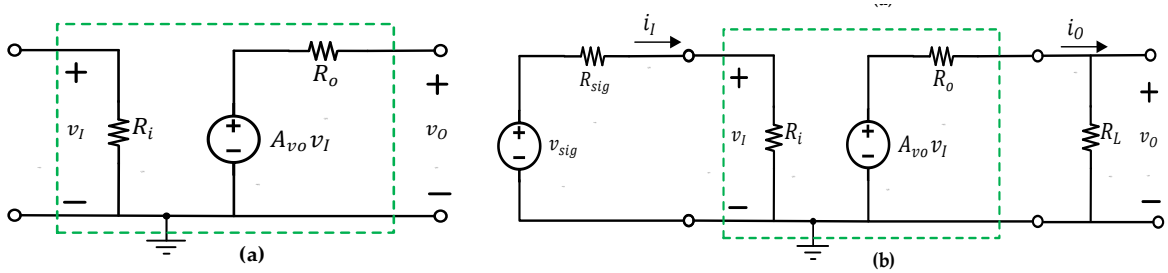


Figure 2: *(a) Circuit model for a voltage amplifier; (b) Voltage amplifier with input signal source and load R_L.*

Figure 2(a) depicts a circuit model for a voltage amplifier. The model includes an input voltage, a control voltage source with gain A_{vo}, an input impedance R_i that causes the amplifier to generate input current from the signal source, and an output impedance R_o that causes leads to a change in output voltage to supply current to a load.

The circuit model in Figure 2(b) illustrates a voltage amplifier supplied by a signal source v_{sig} with source impedance R_{sig} and connected at the output to a load impedance R_L. The non-zero output impedance R_o results in only part of $A_{vo}.v_i$ appearing at the output. Using the voltage division rule, we get [1-5]:

$$v_o = A_{vo} v_i \frac{R_L}{R_L + R_o} \tag{1.1}$$

Thus, the voltage gain is:

$$A_v = \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o} \tag{1.2}$$

To avoid significant gain loss when connecting the amplifier output to the load, R_o should be much smaller than R_L. To maintain a nearly constant output voltage v_o, the amplifier should be designed with R_o much smaller than the minimum R_L value. An ideal voltage amplifier has $R_o = 0$. Equation (1.2) also shows that for $R_L = \infty$, $A_v = A_{vo}$. Hence, A_{vo} is the no-load voltage gain or open-circuit voltage gain of the amplifier.

The input impedance R_i causes a voltage division effect at the input, resulting in only part of the input signal v_{sig} being delivered to the amplifier's input terminal:

$$v_i = v_{sig} \frac{R_i}{R_i + R_{sig}} \tag{1.3}$$

To avoid significant signal loss when connecting the signal source to the amplifier input, the amplifier should be designed with R_i much greater than the source impedance R_{sig}. Furthermore, in many applications where the source impedance varies within a certain range, the amplifier design should ensure R_i is much greater than the maximum value of R_{sig}. An ideal voltage amplifier has $R_i = \infty$. In this ideal case, both current gain and power gain are infinite.

The overall voltage gain (v_o/v_{sig}) can be found by combining equations (1.2) and (1.3):

$$G_v = \frac{v_o}{v_{sig}} = \frac{v_o}{v_i}\frac{v_i}{v_{sig}} = A_{vo} \frac{R_i}{R_i + R_{sig}} \frac{R_L}{R_L + R_o} \tag{1.4}$$

2.3 Analyze CS amplifier stage using MOSFET (NMOS)

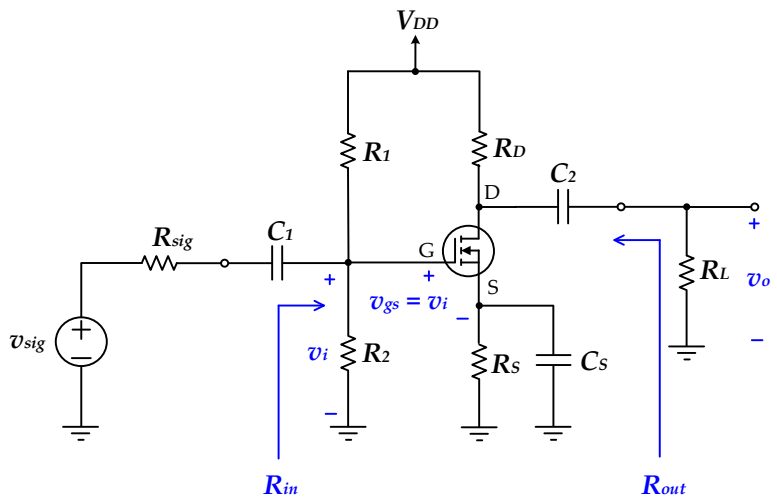


***Figure 3**: Circuit diagram of a single-stage CS voltage amplifier*

In the schematic:

Capacitor C_1 (input coupling capacitor) prevents the internal resistance of the AC signal source from affecting the DC operating point of the amplifier stage (DC isolation between NMOS and input signal source).

Capacitor C_2 blocks DC components from the output stage to the load and passes the AC signal from the output stage to the load (short-circuits AC).

Capacitor C_S short-circuits the source resistor R_S for AC, ensuring the source impedance to ground (0V) is very low. Without C_S, the amplifier gain would be reduced.

Resistor R_S in the source provides DC negative feedback to stabilize the DC operating point of the transistor against temperature variations.

Operating Principle

When an AC signal (short-circuited through capacitor C_1) is applied to the Gate, the Gate voltage varies, causing a corresponding change in the Drain current. This creates an AC voltage across R_D, which is then passed through C_2 to the load R_L.

The small-signal equivalent model (π model) (to calculate AC operating parameters) [1-6]

After biasing the NMOS for active region operation and calculating the DC operating currents I_D, we use the small-signal equivalent model (π model) of the transistor to calculate the AC parameters (gain, input impedance, output impedance) of the amplifier circuit.

- Determine the parameters g_m

$$g_m = \frac{2I_D}{V_{GS} - V_t}$$

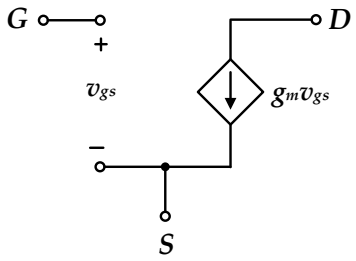


Figure 4. *Small-signal equivalent π model of a MOSFET*

- Convert the circuit diagram Figure 3 to the equivalent diagram Figure 5

In this circuit diagram, because pole S is connected to capacitor C_S, when working in AC mode, pole S will be short-circuited to ground. Then we use the π equivalent model:

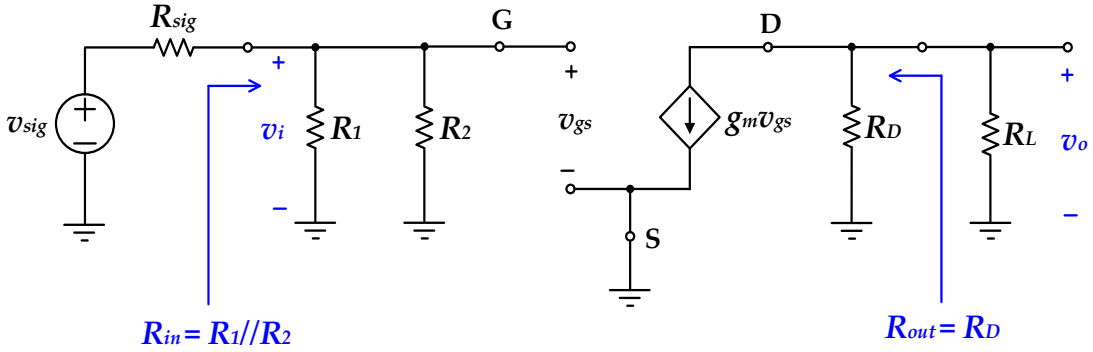


Figure 5*: Equivalent circuit diagram of the amplifier from Figure 3*

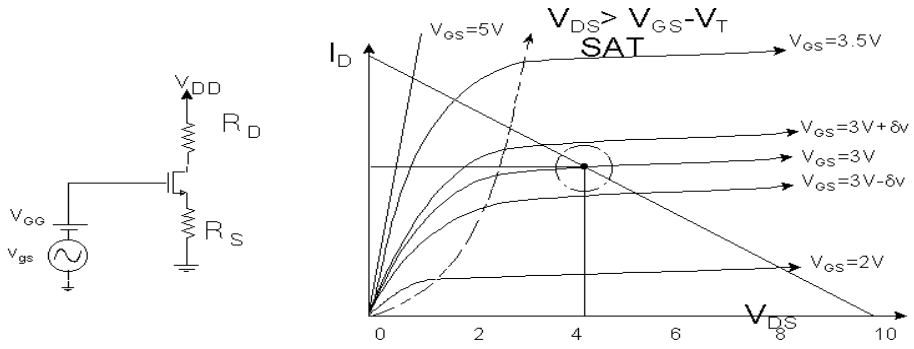
III. DESIGN ILLUSTRATION EXAMPLE

Design of a single-stage amplifier using CS configuration as shown Figure 3 and the equivalent diagram as in Figure 5 that satisfies the following parameters:

- Voltage gain of the circuit: $A_v = -100$
- Load resistor: $R_L = 400\ k\Omega$
- Signal voltage $v_{sig} = 10\ mV$, source impedance $R_{sig} = 50\ \Omega$
- Power supply $V_{DD} = 10\ V$, input impedance R_i, output impedance R_o.
- The circuit's bandwidth is the range of the frequency signal from $f_1 = 100\ Hz$ to $f_2 = 10\ MHz$

Solution

Step 1: Select an appropriate Q point for the Device



- There can be various constraints on selecting the Q point of the device.
- If there is a power constraint that is to be met, then

$$V_{DD} \times I_D = P_{diss}$$

$$I_D < P_{diss}/V_{DD}$$

- Since this constraint is not mentioned, for this problem, we will choose the following:

$$V_{DSQ} = 4V; I_D = 1\ mA; V_{DSQ} > \text{approx}\ V_{DD}/3 \text{ to } V_{DD}/2$$

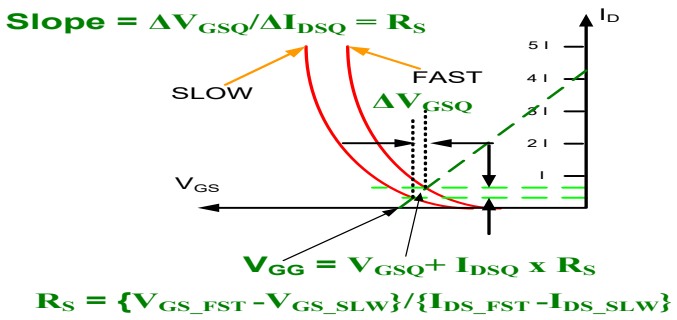
- In general

$$V_{DD} = I_D R_D + V_{DSQ} + I_D R_S \tag{1.5}$$

$$\text{If} \quad V_{DSQ} = V_{DD}/2 \tag{1.6}$$

$$I_D < \frac{V_{DD}}{2(R_D + R_S)} \tag{1.7}$$

Step 2: Determine R_S from I_D vs V_{GS} curve of the given Mosfet.



From the above curve Rs = 2KΩ.

Step 3: Determine R_D from the given gain specification.

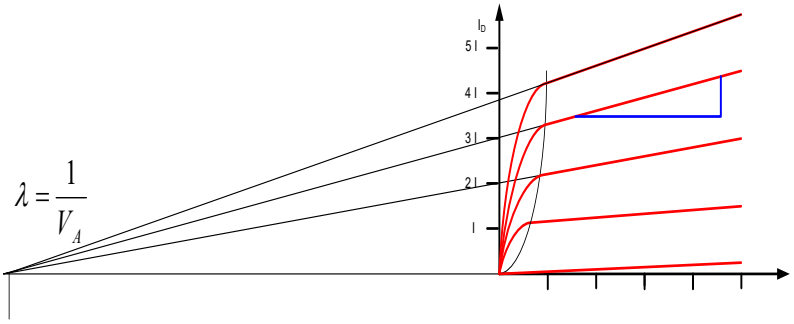
The DC gain of the given circuit can be expressed as

$$A_v = -g_m(R_D \| r_o \| R_L) = -100 \tag{1.8}$$

- Since we have chosen the required current, r_o can be calculated from

$$r_o = \frac{1}{\lambda I_D}$$

- If λ is not mentioned it can be calculated from the given I_D –V_{DS} curves of the transistor



- g_m can be calculated from I_D vs V_{GS} curve of the device as

$$Slope = \Delta I/\Delta V_{GS} = g_m = \beta \Delta V = I_D 2/\Delta V$$

If $R_D \ll r_o, R_L$ then Eq (1.8) can be expressed as

$$A_v = -g_m \times R_D = -10$$

Assuming $g_m = 1\ mS$, R_D can be calculated to be equal to 10 KΩ. $R_{out} \approx R_D$

Step 4: Determine the required V_{GG}

$$V_{GG} = V_{GS} + I_D R_S = 3\ V + 1\ mA \times 2\ k\Omega = 5\ V$$

The value of V_{GS} was chosen from curve 1.

Step 5:

$$V_{GG} = \frac{R_2}{R_1 + R_2} V_{DD}$$

Choose

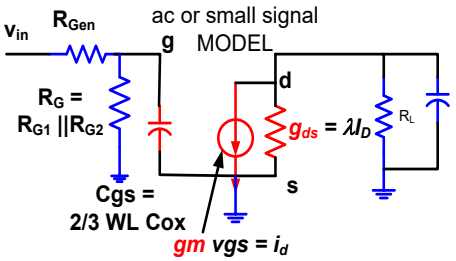
$$R_G = R_1 \| R_2 \gg R_{sig}.$$

$$R_{in} = R_G$$

R_{sig} for most instruments is 50Ω, choosing $R_1 = R_2 = 10\ M\Omega$

So, we have $R_G = 5\ M\Omega$ and $V_{GG} = 5\ V$.

Step 6: From the small signal model of the amplifier, determine the poles



$$v_o(g_{ds} + R_L) + v_o s C_L + g_m v_g = 0$$

$$v_o = -g_m v_g/\{(g_{ds} + R_L) + v_o s C_L\} \approx -g_m R_L v_g/\{1 + sR_L C_L\}$$

$$v_g(R_{sig} + R_G + sC_{gs}) - v_{in} R_{sig} = 0$$

$$v_g = v_{in} R_{sig}/(R_{sig} + R_G + sC_{gs})$$

$$v_g \approx v_{in} R_{sig}/(R_{sig} + sC_{gs}) = 1/(1 + sR_{sig} C_{gs})$$

The following are the "f_l" poles of the circuit.

$$P_1 = \frac{1}{2\pi(R_G + R_{sig})C_1} \approx \frac{1}{2\pi(R_{sig})C_1}$$

$$10\ Hz < \frac{1}{2\pi(5000 + 50)C_1}$$

$C_1 > 3.15\ \mu F$, choose $C_1 = 4.7\ \mu F$

$$P_2 = \frac{1}{2\pi R_S C_S}$$

$C_S > 8\ \mu F$, choose $C_S = 10\ \mu F$

$$P_3 = \frac{1}{\{2\pi(R_D \| r_{DS} + R_L)\}C_2} \approx \frac{1}{2\pi(R_L)C_2}$$

$C_2 > 38\ nF$, choose $C_2 = 47\ \mu F$

$$P_4 = \{g_{DS} + R_D + G_L\}/\{2\pi C_L\}$$

$$P_4 \approx \frac{1}{2\pi(R_D)C_L}$$

In many cases

$C_L < 3\ pF$, choose or make sure that is $C_L < 3\ pF$ or is selected at $C_L = 2\ pF$

$$P_5 = \frac{1}{2\pi(R_{sig})C_{gs}}$$

When using a discrete device, check data sheet to make sure CISS meets the criteria for P5.

IV. SIMULATION RESULTS AND DISCUSSION

4.1. Simulation of DC mode

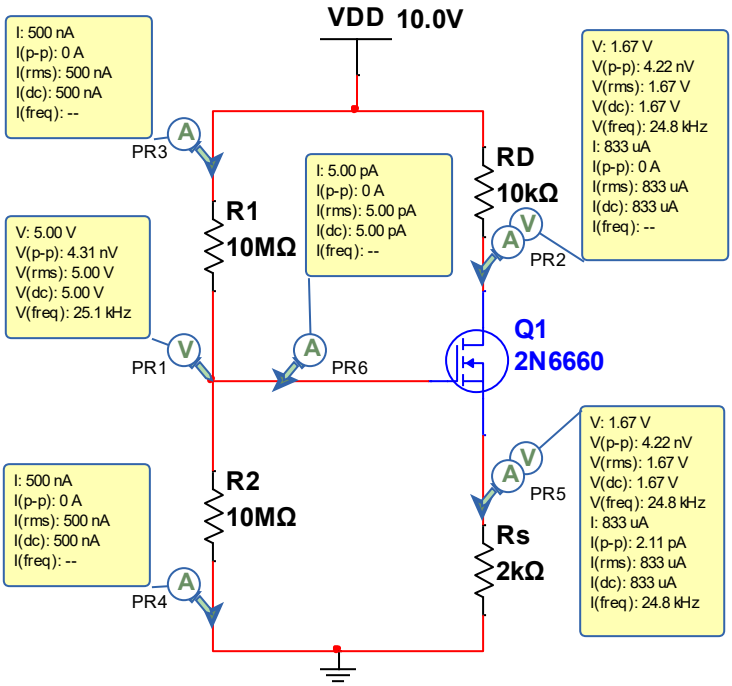


Figure 6: *DC bias circuit simulation diagram*

Remarks

Measured DC current and voltage values: $V_{GG} = 5\ V;\ V_D = 1.67V\ ; V_S = 1.67V$

$I_G = 5\ pA\ ; I_D = I_S = 833\ \mu A$

These measured values are approximately the calculated values.

4.2. Simulation of AC small signal

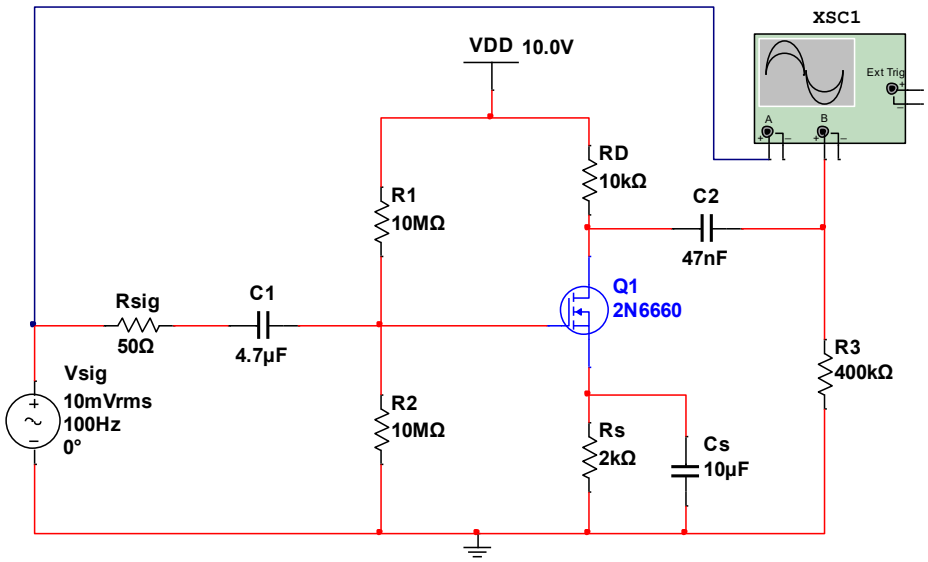


Figure 7: *Simulation diagram when* $R_L = 400\ k\Omega$

The result of input-output waveform of amplifier circuit

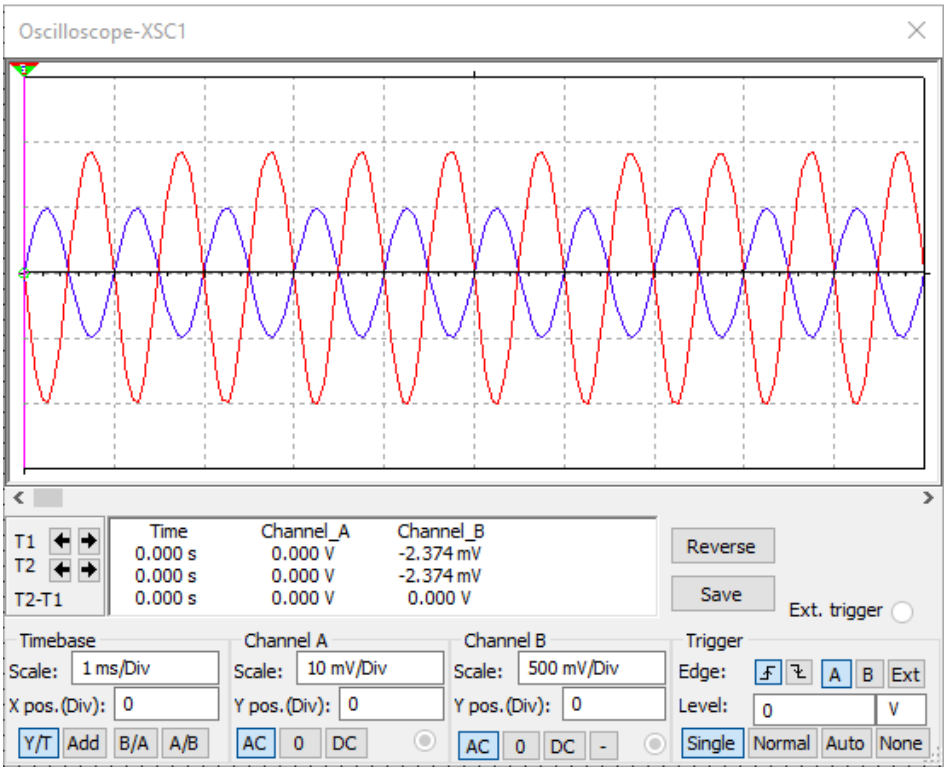


Figure 8: *The output waveform result (blue: input voltage, red: out voltage)*

Remarks

The waveform in Figure 11 also clearly reveals a phase shift of 180° between input and output voltages.

Voltage gain*:* $A_V \cong 940\ mV/10\ mV = 94$

From the simulation diagrams of Figure 7 and Figure 8, we see that the voltage gain A_V when having load is approxiate the desired voltage gain A_V =100.

V. CONCLUSION

The design and simulation of the single-stage CS amplifier using a voltage-divider biased MOSSFET transistor provides a clear methodology for developing efficient amplifier circuits. The simulation results validate the theoretical calculations and demonstrate the feasibility of the design approach

Acknowledgments

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