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# Design and simulation of audio frequency amplifier using BJT transistor

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***Abstract***
*Signal amplification is an indispensable step in electronic circuits because it is impractical to use direct signals from sensors to control devices without an amplifier circuit. Some input signals are very small and need amplification to be large enough to affect the circuit and control devices. In this paper, we present the steps to design a single-stage Common Emitter (CE) amplifier using a voltage-divider biased BJT transistor [1-5]. After analyzing and calculating the DC and AC operation modes of the amplifier circuit, we proceed to simulate it on Multisim software to verify the theoretical results. The example in this article can also serve as reference materials for electrical and electronics students in technical universities.*

***Keywords:*** *amplifier, audio frequency amplification, bias, BJT transistor, Multisim.*

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## I. INTRODUCTION

Amplification is a controlled energy conversion process, where the energy of a DC power supply (which does not contain information) is converted into AC energy (with transformation rules that carry the required information). In other words, this is an analog signal processing process. The article provides basic knowledge of a voltage amplifier, analysis of a single-stage CE amplifier circuit using BJT transistors connected in a voltage divider configuration. We then take an example to illustrate the steps to design an audio frequency amplifier circuit with some given parameters.

## II. THEORETICAL BASIS

### 2.1. General Introduction to Amplification

An amplifier is used to convert relatively "weak" signals, i.e., in the range of microvolts (μV) or millivolts (mV) and with low energy, into signals with larger amplitude [1-5]

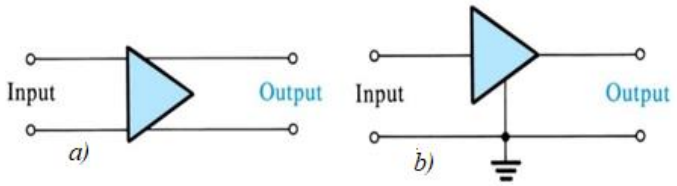


***Figure 1*****:** *(a) Schematic symbol of an amplifier circuit; (b) Amplifier with a common point (ground) between the input and output ports.*

### 2.2 Voltage Amplifier

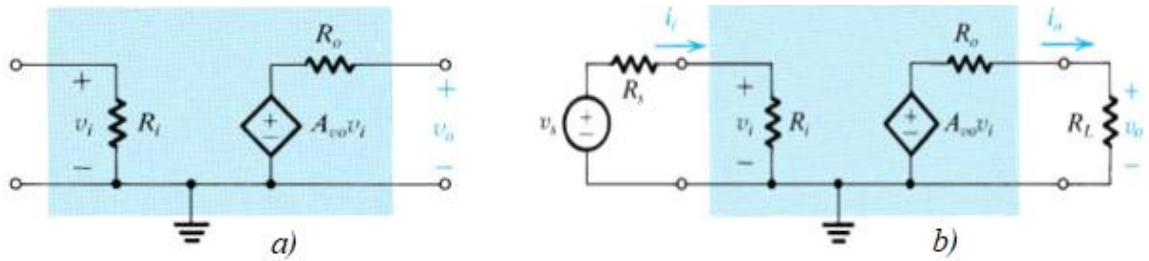


***Figure 2**: (a) Circuit model for a voltage amplifier; (b) Voltage amplifier with input signal source and load.*

Figure 2(a) depicts a circuit model for a voltage amplifier. The model includes an input voltage, a control voltage source with gain $A_{vo}$, an input impedance $R_i$ that causes the amplifier to generate input current from the signal source, and an output impedance $R_o$ that causes leads to a change in output voltage to supply current to a load.

The circuit model in Figure 2(b) illustrates a voltage amplifier supplied by a signal source $v_s$ with source impedance $R_s$ and connected at the output to a load impedance $R_L$. The non-zero output impedance $R_o$ results in only part of $A_{vo}.v_i$ appearing at the output. Using the voltage division rule, we get [1-5]:

$$v_o = A_{vo}v_i \frac{R_L}{R_L + R_o} \tag{1.1}$$

Thus, the voltage gain is:

$$A_v = \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o} \tag{1.2}$$

To avoid significant gain loss when connecting the amplifier output to the load, $R_o$ should be much smaller than $R_L$. To maintain a nearly constant output voltage $v_o$, the amplifier should be designed with $R_o$ much smaller than the minimum $R_L$ value. An ideal voltage amplifier has $R_o = 0$. Equation (1.2) also shows that for $R_L = \infty$, $A_v = A_{vo}$. Hence, $A_{vo}$ is the no-load voltage gain or open-circuit voltage gain of the amplifier.

The input impedance $R_i$ causes a voltage division effect at the input, resulting in only part of the input signal $v_s$ being delivered to the amplifier's input terminal:

$$v_i = v_s \frac{R_i}{R_i + R_s} \tag{1.3}$$

To avoid significant input signal loss when connecting the signal source to the amplifier input, the amplifier should be designed with $R_i$ much greater than the source impedance $R_s$. Furthermore, in many applications where the source impedance varies within a certain range, the amplifier design should ensure $R_i$ is much greater than the maximum value of $R_s$. An ideal voltage amplifier has $R_i = \infty$. In this ideal case, both current gain and power gain are infinite.

The overall voltage gain ($v_o/v_s$) can be found by combining equations (1.2) and (1.3):

$$G_v = \frac{v_o}{v_s} = \frac{v_o}{v_i}\frac{v_i}{v_s} = A_{vo} \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o} \tag{1.4}$$

### 2.3 Analyze CE amplifier stage using BJT

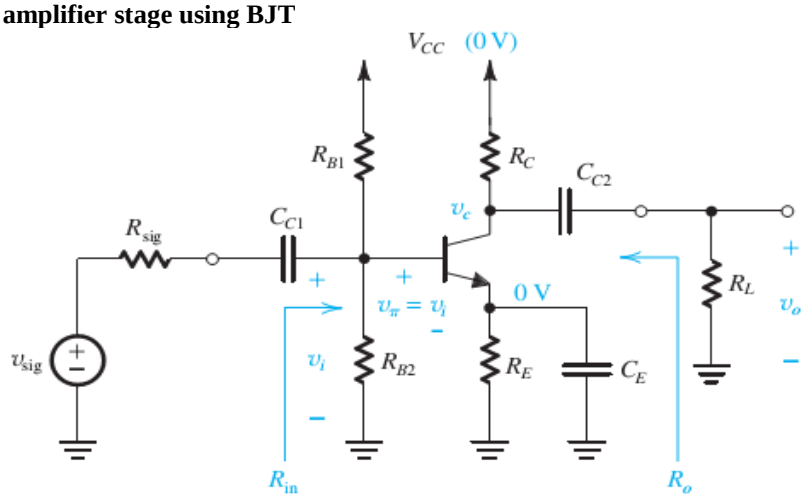


***Figure 3**: Circuit diagram of a single-stage CE voltage amplifier*

***In the schematic:***

Capacitor $C_{C1}$ (input coupling capacitor) prevents the internal resistance of the AC signal source from affecting the DC operating point of the amplifier stage (DC isolation between BJT and input signal source).

Capacitor $C_{C2}$ blocks DC components from the output stage to the load and passes the AC signal from the output stage to the load (short-circuits AC).

Capacitor $C_E$ short-circuits the emitter resistor $R_E$ for AC, ensuring the emitter impedance to ground (0V) is very low. Without $C_E$, the amplifier gain would be reduced.

Resistor $R_E$ in the emitter provides DC negative feedback to stabilize the DC operating point of the transistor against temperature variations.

***Operating Principle***

When an AC signal (short-circuited through capacitor $C_{C1}$) is applied to the base, the base current varies, causing a corresponding change in the collector current. This creates an AC voltage across $R_C$, which is then passed through $C_{C2}$ to the load.

***Votage divider bias (to calculate DC operating point) [1-5]***

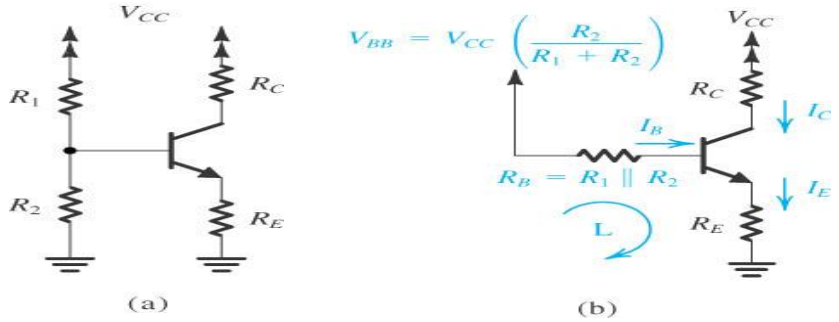


***Figure 4****: Voltage divider bias*

***The small-signal equivalent model (π model) (to calculate AC operating parameters) [1-5]***

After biasing the BJT for active region operation and calculating the DC operating currents $I_C$ and $I_E$, we use the small-signal equivalent model (π model) of the transistor to calculate the AC parameters (gain, input impedance, output impedance) of the amplifier circuit.

- Determine the parameters $g_m$ và $r_\pi$ , $r_o$: (assume $r_o$ is very large so it should be ignored)

$$g_m = I_C/V_T;\ r_\pi = \beta/g_m = V_T/I_B$$

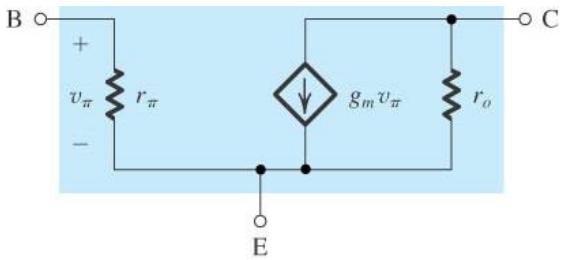


***Figure 5.*** *Small-signal equivalent π model of a BJT*

- Convert the circuit diagram Figure 3 to the equivalent diagram Figure 6

In this circuit diagram, because pole *E* is connected to capacitor $C_E$, when working in AC mode, pole E will be short-circuited to ground. Then we use the π equivalent model:

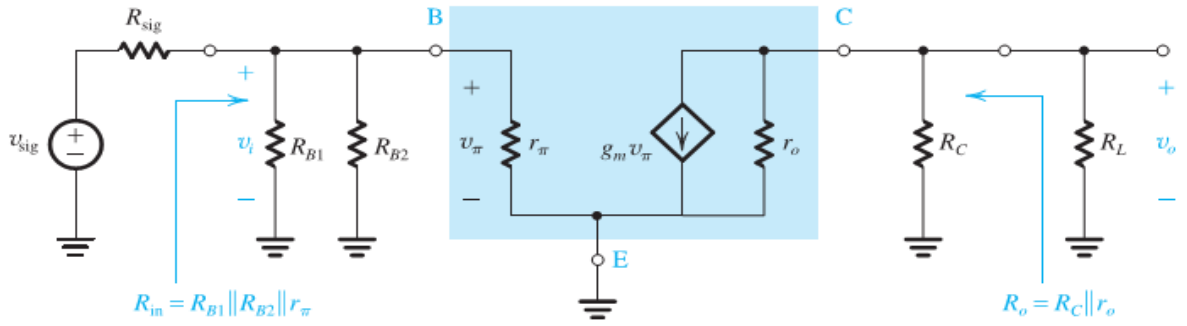


***Figure 6**: Equivalent circuit diagram of the amplifier from Figure 3*

## III. DESIGN ILLUSTRATION EXAMPLE

Design of audio frequency amplifier using CE configuration as shown Figure 3 and the equivalent diagram in Figure 6 that satisfies the following parameters:

- Voltage gain of the circuit at no load: $A_v = 100$
- Input voltage $v_{in} = 10\ mV$, source impedance $R_{sig} = 100\ \Omega$
- Power supply $V_{CC} = 15\ V$, input impedance $R_i$, output impedance $R_o$.
- The circuit's bandwidth is the range of the audio frequency signal from 20Hz - 20kHz

**Solution**

Step 1: Choose BJT type 2N2222 (look up datasheet), with the following parameters:

$$V_{BE} = 0.65\ V;\ I_C = 4\ mA;\ \beta = 180$$

Step 2: Select $V_{CC} = 15\ V$, calculate the DC current and voltage on the transistor terminals to find the DC operating point Q.

To ensure the best amplification mode (class A), the dc operating point *Q* is usually chosen in the middle of the dc load line:

$$I_{CQ} \approx 0{,}5\ I_{C(short-circuit)};\ V_{CEQ} \approx 0{,}5\ V_{CE(open-circuit)}$$

The no-load gain $A_V$ is calculated: $A_V = -g_m.R_C = 100$ with $g_m = I_C/V_T = 4\ mA/25\ mV = 0.16\ A/V$

Step 3: Choose $R_C$. Can be calculated: $R_C = 100/g_m = 100/0.16\ (A/V) \cong 0.63\ k\Omega \rightarrow$ Choose $R_C = 1\ k\Omega$

Step 4: Choose $R_E$. The voltage value $V_E$ is usually chosen: $V_E = (0.1\ \div 0.3)V_{CC} \cong 4\ V$

$V_E = I_E.R_E = 4\ V$. Choose $R_E = 1\ k\Omega$

Step 5: Choose $R_{B1}, R_{B2}$

$V_B = V_{BE} + V_E = 0.65\ \text{V} + 4\ V = 4.65\ V$

$V_{BB} = \frac{R_{B2}}{R_{B1}+R_{B2}} V_{CC} = 4.65\ V \Rightarrow \frac{R_{B2}}{R_{B1}+R_{B2}} = \frac{4.65\ V}{15\ V} = 0.31$. Choose $R_{B1} = 10\ k\Omega$; $R_{B1} = 4.7\ k\Omega$

$V_C = V_{CC} - I_C.R_C = 15\ \text{V} - (4\ \text{mA} \times 1k\Omega) = 15\ V - 4\ V = 11\ V$

$V_{CE} = V_C - V_E = 11\ V - 4\ V = 7\ V$

DC load line equation: $V_{CE} = V_{CC} - I_C(R_C + R_E)$

- ✓ Open - circuit point: $I_C = 0 \rightarrow V_{CE} = V_{CC} = 15\ V$
- ✓ Short - circuit point: $V_{CE} = 0\ V \rightarrow I_C = V_{CC}/(R_C + R_E) = 15 \frac{\text{V}}{1\ k\Omega + 1\ k\Omega} = 7.5\ \text{mA}$

The DC operating point Q: $(I_{C_Q}, V_{CE_Q}) = (4\ mA; 7\ V)$

Calculate some parameters:

$$R_B = (R_{B1} \| R_{B2}) = \frac{R_{B1}.R_{B2}}{R_{B1} + R_{B2}} = \frac{10k\Omega \times 4.7\ k\Omega}{10k\Omega + 4.7\ k\Omega} \cong 3.2k\Omega$$

$$r_\pi = \beta/g_m = 180/0.16\ A/V \approx 1{,}13k\Omega$$

Input impedance $R_{in}$

$$R_{in} = R_B \| r_\pi = \frac{R_B.r_\pi}{R_B + r_\pi} \cong r_\pi = 1{,}13k\Omega$$

The input impedance $R_{in}$ of the CE amplifier stage is not exceeded 1 ÷ 3 kΩ.

Output impedance $R_o$

$$R_O = R_C \| r_o = \frac{R_C.r_O}{R_C + r_O} \approx R_C = 1k\Omega$$

The amplifier input voltage $v_{in}$ is calculated:

$$v_{in} = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig} = \frac{1{,}13k\Omega}{1{,}13\ k\Omega + 0{,}1\ k\Omega} 10\ mV \cong 9{,}2\ mV$$

The amplifier output voltage $v_o$ is calculated:

$$v_O = -g_m v_{in}(R_o \| R_L) = -g_m v_{in} \frac{R_O R_L}{R_O + R_L}$$

Substituting the expression $v_{in}$ into the expression $v_O$, we get:

$$v_O = -g_m v_{sig} \frac{R_{in}}{R_{in} + R_{sig}} \frac{R_O . R_L}{R_O + R_L} = 1227mV = 1{,}227V$$

The voltage gain of the amplifier circuit is:

$$G_v = \frac{v_O}{v_{sig}} = -g_m \frac{R_{in}}{R_{in} + R_{sig}} \frac{R_O . R_L}{R_O + R_L} = 135$$

(The negative sign in the equation for $G_v$ clearly reveals a phase shift of 180° between input and output voltages).

Step 6: Choose capacitor parameters: $C_1$; $C_2$; $C_E$

The audio frequency signal with $\omega_L = 20\ Hz$. The $C_E$ capacitor value is usually chosen to be 80% $\omega_L$

$C_E$ is calculated according to: $1/C_E . R_E = 0.8 \times 2\pi f_{p_3}$

$R_E$ is calculated $R_E = r_E + \frac{R_B \| R_{sig}}{1+\beta} = \frac{V_T}{I_E} + \frac{R_B \| R_{sig}}{1+\beta} \cong 0.8\ k\Omega$

Calculated: $C_E$ = 420,437 µF. Choose $C_E$ = 420µF

The $C_1$ capacitor value is usually chosen to be 10% $\omega_L$. $C_1$ is calculated according to: $1/C_1 . R_{C1} = 0.1 \times 2\pi f_{p_1}$

$R_{C1}$ is calculated: $R_{C1} = (R_B \| r_\pi) + R_{sig} \cong 1.2\ k\Omega$. Caculated $C_1 = 66.24\ \mu F$. Choose $C_1 = 66\ \mu F$

The $C_2$ capacitor value is also chosen to be 10% $\omega_L$. $C_2$ is calculated according to: $1/C_2 . R_{C2} = 0.1 \times 2\pi f_{p_2}$

$R_{C2}$ is calculated: $R_{C2} = R_C + R_L = 6\ k\Omega$. Caculated $C_1 = 13.27\ \mu F$. Choose $C_2 = 13\ \mu F$

## IV. SIMULATION RESULTS AND DISCUSSION

### 4.1. Simulation of DC mode

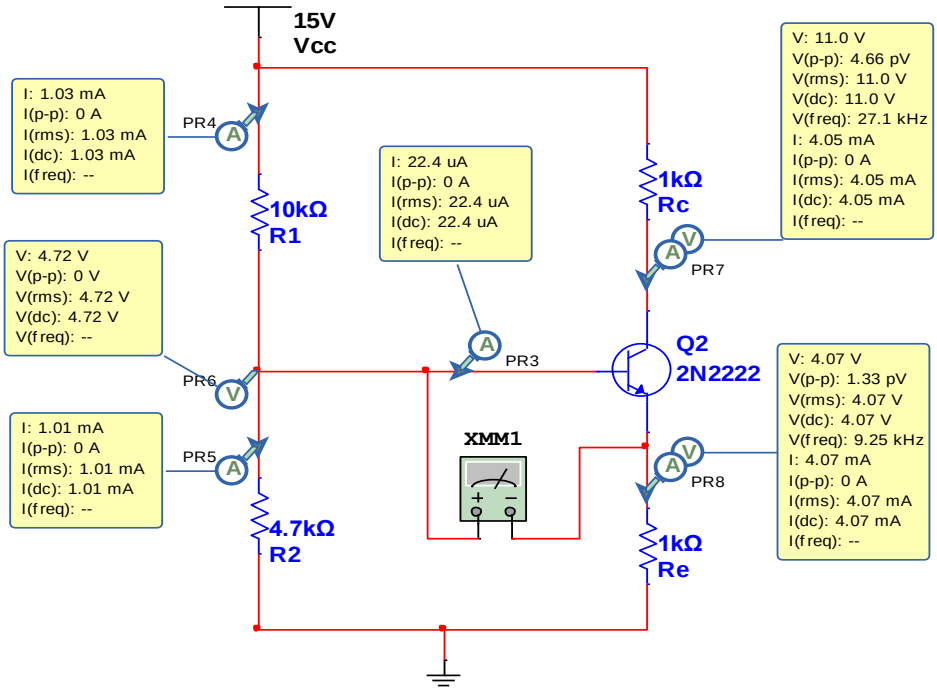


***Figure 7:*** *DC bias circuit simulation diagram*

***Remarks***

Measured DC current and voltage values: $V_B = 4.72V;\ V_C = 11V\ ;V_E = 4.07V$

$I_B = 22.4\mu A\ ; I_C = 4.05mA\ ; I_E = 4.07mA$

These measured values are approximately the calculated values.

### 4.2. Simulation of AC small signal

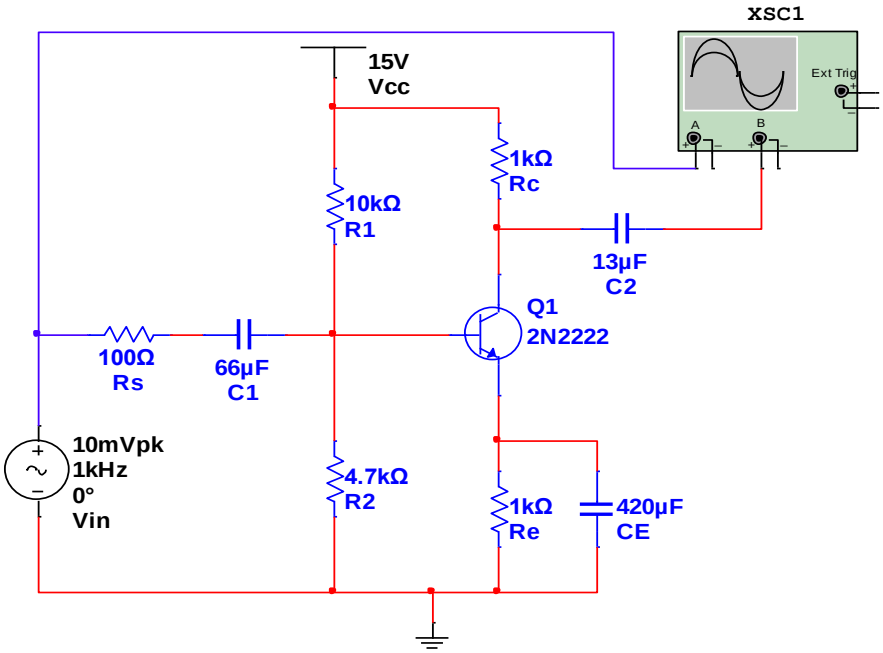


***Figure 8**: Simulation diagram when no load $R_L$*

***The result of input-output waveform of amplifier circuit***

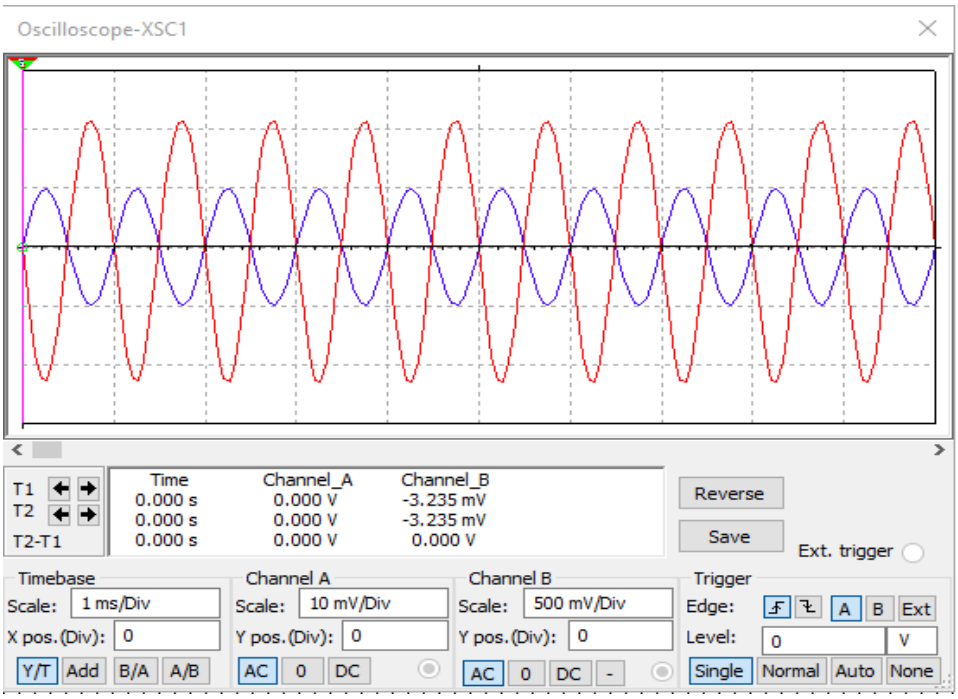


***Figure 9:** Output waveform results when no load $R_L$ (blue: input voltage; red: output voltage)*

***Remarks***

The waveform in Figure 9 clearly reveals a phase shift of 180° between input and output voltages.

Voltage gain when no load $R_L$: $A_V \cong 1100\ mV/10\ mV = 110$

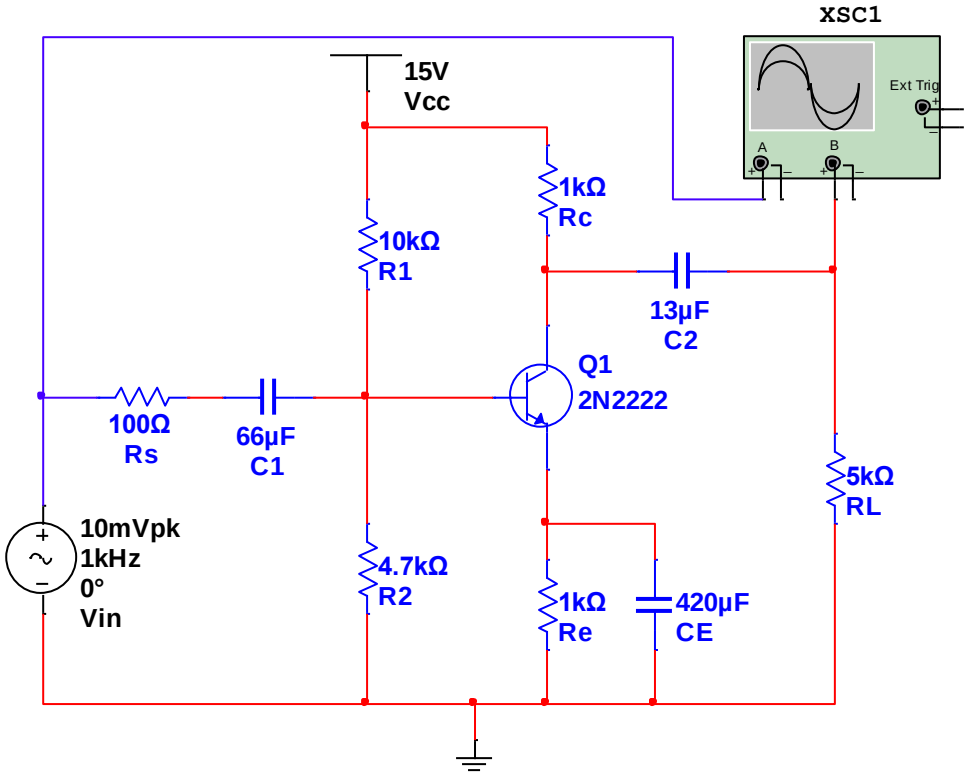


***Figure 10:*** *Simulation diagram when having load ($R_L = 5\ k\Omega$)*

***The result of input-output waveform of amplifier circuit***

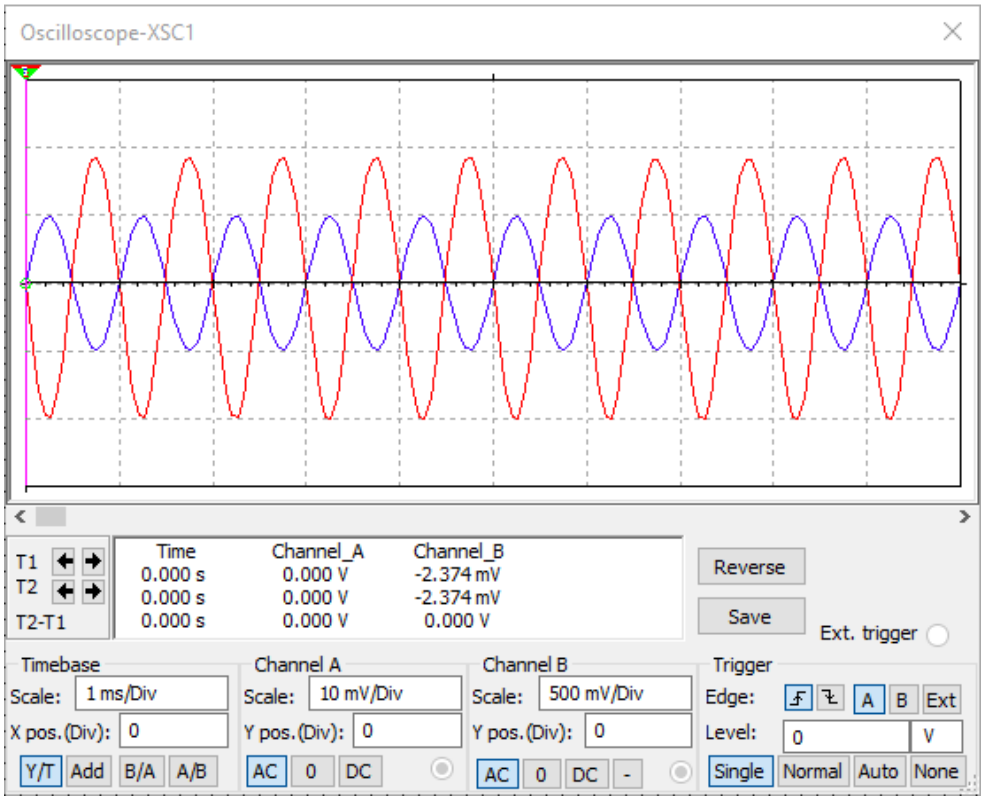


***Figure 11:*** *Output waveform results when having load $R_L$ (blue: input voltage, red: out voltage)*

***Remarks***

The waveform in Figure 11 also clearly reveals a phase shift of 180° between input and output voltages.

Voltage gain when having load $R_L$**:** $A_V \cong 950\ mV/10\ mV = 95$

From the simulation diagrams of Figure 9 and Figure 11, we see that the voltage gain $A_V$ when no load is larger than the voltage gain $A_V$ when having load.

## V. CONCLUSION

The design and simulation of the single-stage CE amplifier using a voltage-divider biased BJT transistor provide a clear methodology for developing efficient amplifier circuits. The simulation results validate the theoretical calculations and demonstrate the feasibility of the design approach

## Acknowledgments

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