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Space vector Pulse width modulation of Five phase supply for Three Level inverter with sample reference phase voltage

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Abstract: *A simplified three-level, five-phase space vector pulse width modulation (SVPWM) is suggested. Based on dwell times of the two-level inverter and the duty cycle of the three-level inverter switches, the proposed method index of carriers. Based on the modulation index, the suggested approach automatically selects the eligible vectors, region, and switching order of the five optimized vectors. In order to generate the necessary voltage reference in the main subspace and zero the average voltage in the auxiliary subspace, 113 of the most eligible vectors, out of a total of 243 available vectors, are used. The redundant vectors in each subcycle are also used in this way, balancing the dc-link capacitor voltages without the need for an additional algorithm or technique. The proposed approach can be simply expanded for any multiphase multilevel (5, 7,..., n) inverter by merely modifying the carrier index. The simulation of three-level five-phase inverter support the proposed approach.*

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I. Introduction

Due to their benefits including low output harmonics in the voltage and current, low switching loss, reduced dv/dt, and reduced common mode voltage [1]–[3], MULTILEVEL inverters are suggested as an alternative for medium- and high-power applications in industries. The advantages of multiphase drives over conventional three-phase drives, such as higher fault tolerance, reduced amplitude and increased frequency of torque pulsation, reduced dc-link current harmonics, reduced size due to higher power density, and reduced current per phase, have led to increased interest in applications such as ship propulsion, electric traction, hybrid, and electrical vehicles [4]–[6]. Consequently, the multilayer multiphase drives have both of the aforementioned benefits. Major research efforts have concentrated on creating space vector pulse width modulation (SVPWM) for multiphase driving systems. In [7], a method for producing sinusoidal voltage devoid of lower-order harmonics is suggested. This method involves bringing the average voltage in the auxiliary subspace to zero by applying the big vector 1.618 times greater than the medium vector.time vector for each sampling period. In [8], an SVPWM method based on the unified method is proposed for the nine-phase two-level inverter by centering the active vectors by offset addition. An approach based on the three nearest vectors was put out in [9] for three-level, five-phase applications, but it ignores the auxiliary subspace. An SVPWM technique for a three-level, five-phase system is proposed in [10] with the goal of decreasing torque ripple using a "walking pattern" to pick the vectors. The simulation and prototype results for different modulation index are presented, and this validates the effectiveness of the proposed implementation technique.

II. THREE-LEVEL FIVE-PHASE DIODE CLAMPED INVERTER

Fig. 1 depicts the hardware topology of a three-level, five-phase inverter. It has five legs, and each leg contains four switches that can only be controlled in pairs that are two complimentary to one another. One complementary pair of switches, Sx1 and S'x1 (x = A,B,C,D,E), and the other, Sx2 and S'x2, are available. By regulating the four switches listed in Table I, each leg voltage can be brought to one of three voltage levels. Thus, there are a total of 3 x 5 = 243 switching states that could occur. There are 240 nonzero and 3 zero vectors among

them. There are now only 113 qualifying vectors left in existence. Sector-I is used as an example case throughout this paper to demonstrate the validity of the algorithm; similarly, it may be demonstrated for other sectors. In Sector-I, a total of 21 vectors are eligible.Figure 2. shows the ideal switching order in Region F1 with zero vectors. As seen in Fig. 2, dotted red lines split each sector into subregions. Fig. 3 displays the ideal five vector switching order in Region F1 based on [12].

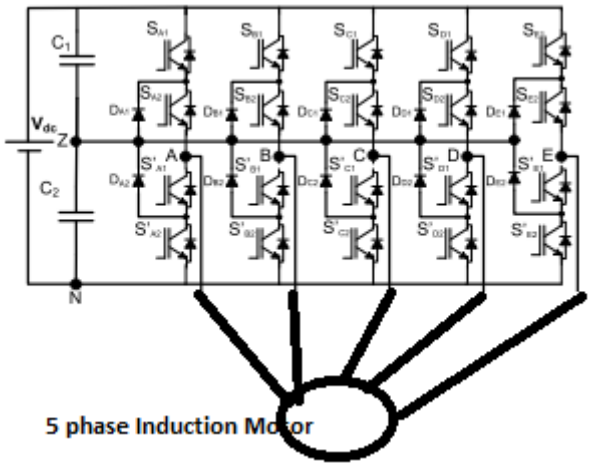

Fig.1 Three Level Five phase Inverter

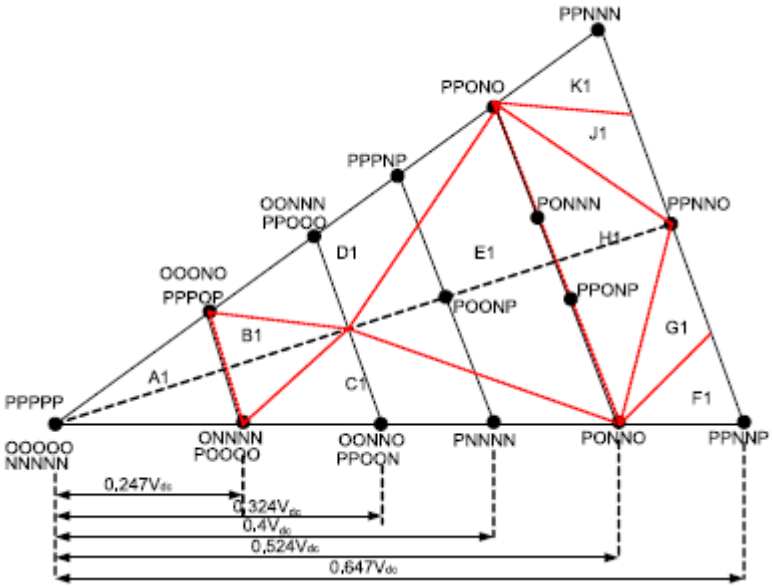

Fig 2: Eligible Vectors

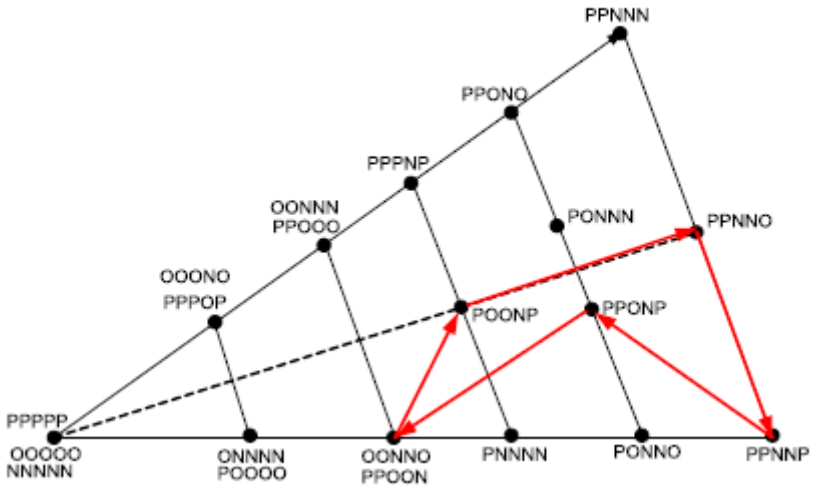

Fig 3 :Optimum Switching Sequence of Region 1

III. MAPPING OF TWO-LEVEL DWELL TIME TO THREE-LEVEL

A.Dwell Time calculations

In light of the two-level stay time and reference stage voltage transporter record, the stay season of the three-level inverter can be gotten. The two-level stay time can be found out
by a straightforward strategy as determined. The age of the transporter record from the reference voltage is made sense of in following area.

$$T_a = \frac{2^*V_{\mathrm{AO}}}{V_{\mathrm{dc}}}T_s; T_b = \frac{2^*V_{\mathrm{BO}}}{V_{\mathrm{dc}}}T_s; T_c = \frac{2^*V_{\mathrm{CO}}}{V_{\mathrm{dc}}}T_s;$$

$$T_d = \frac{2^*V_{\mathrm{DO}}}{V_{\mathrm{dc}}}T_s; T_e = \frac{2^*V_{\mathrm{EO}}}{V_{\mathrm{dc}}}T_s \quad (1)$$

$$T_{\mathrm{eff}} = T_{\max} - T_{\min} \quad (2)$$

$$T_{\max} = \mathrm{Max}(T_a, T_b, T_c, T_d, T_e) \quad (3)$$

$$T_{\min} = \mathrm{Min}(T_a, T_b, T_c, T_d, T_e) \quad (4)$$

$$T_{\mathrm{offset}} = \frac{1}{2}\left(2^*T_s - (T_{\max} - T_{\min})\right). \quad (5)$$

*V*AO, *V*BO, *V*CO, *V*DO, and *V*EO are sampled amplitudes of the reference voltage of phases A, B, C, D, and E, respectively, *Ts* is the sampling time period, and *T*eff is the effective time. The switching time obtained by (1) could be negative if reference voltage is negative. In order to eliminate the negative time of switches, an offset has to be added based on the effective time and it is given by (5).

$$T_{ga} = \frac{2^{*}V_{AO}}{V_{\mathrm{dc}}} T_s + T_{\mathrm{offset}}$$

$$T_{gb} = \frac{2^{*}V_{BO}}{V_{\mathrm{dc}}} T_s + T_{\mathrm{offset}}$$

$$T_{gc} = \frac{2^{*}V_{CO}}{V_{\mathrm{dc}}} T_s + T_{\mathrm{offset}}$$

$$T_{gd} = \frac{2^{*}V_{DO}}{V_{\mathrm{dc}}} T_s + T_{\mathrm{offset}}$$

$$T_{ga} = \frac{2^{*}V_{AO}}{V_{\mathrm{dc}}} T_s + T_{\mathrm{offset}}.$$

In view of the two-level exchanging time and transporter file, the rationale for planning two-level changing state to three-level exchanging state as made sense of in Segment can be summed up as truth table. In view of the above truth table, planning of two-level exchanging state to three level is made sense of for all the five-stage graphically for two cases in Area I. The stage voltage relationship in Area I is displayed in Fig. 4.

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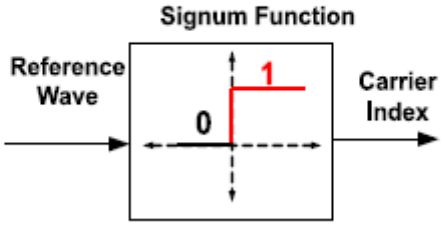

Fig 4. Carrier Index generation

IV. Validation of the Algorithm for the Optimal Five-Vector Switching Strategy

Themapping of the exchanging state for the three-level inverter in light of the two-level exchanging state consequently chooses the OFV in light of the regulation record is 1, the reference vector is in Area I and in the District F1. According to ,the ideal five-vector exchanging procedure is displayed in the Fig. 3 by red lines with arrow points. The TABLE III

Ideal FIVE-VECTOR Exchanging Arrangement IN Area I Subregion Inverter states utilized during exchanging grouping

1 (A1) OONNO-OOONO-OOOOO-POOOO-PPOOO-PPOOP
2 (B1) OONNO-OOONO-POONO-POOOO-PPOOO-PPOOP
3(C1) OONNO-PONNO-POONO-POOOO-PPOOO-PPOOP
4 (D1) OONNO-PONNO-POONO-PPONO-PPOOO-PPOOP
5 (E1) OONNO-OOONO-POONO-PPONO-PPOOO-PPOOP
6 (F1) OONNO-PONNO-PPNNO-PPNNP-PPONP-PPOOP
7(G1) OONNO-PONNO-PPNNO-PPONO-PPONP-PPOOP
8(H1) OONNO-PONNO-PPNNO-PPONO-PPOOO-PPOOP
9(I1) OONNN-PONNN-PONNO-PPNNO-PPONO-PPOOO
10(J1) OONNN-PONNN-PPNNN-PPNNO-PPONO-PPOOO

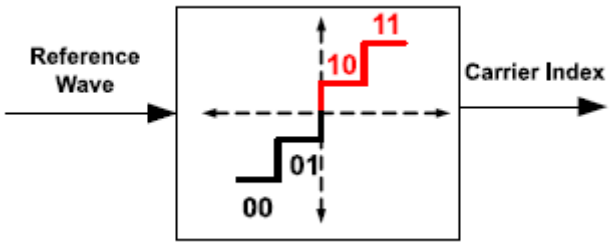

Fig.5. Carrier index generator for five level.

V. SIMULATION RESULTS

Initially, to verify the proposed algorithm, the simulations are made with the help of MATLAB SIMULINK blocks and Sfunctions to generate the gate pulse for the five-phase three-level inverter. The parameters used for the simulation are: *V*dc = 220 V, the value of dc-link capacitors are C1 , *C*2 = 1200 uF/350 V with ESR of 0.05 Ω and *RL* load is used with *R* = 450 Ω, *L* = 600 mH per phase. The output frequency (*f*) of the inverter is 50 Hz, the witching frequency is *fs* = 4 kHz, and the sampling interval *Ts* is 0.25 ms. For simulation, the dead time between the complementary switches is not considered. The adjacent line voltage is used as the line voltage throughout this paper. Fig. 11 shows the phase and line voltage obtained from simulation for the modulation index (MI) = 1 using the simplified SVPWM method for the three-level five-phase inverter. Fig. 12 shows the simulated harmonic spectrum of the line current waveform for MI = 1. The low-order harmonics in the line current is around 0.2% of the fundamental. The dc-link capacitors voltage variation for MI = 1 in C1 and C2 is around 0.02 V. The dc-link capacitor variation for MI = 0.4 is shown in Fig.8

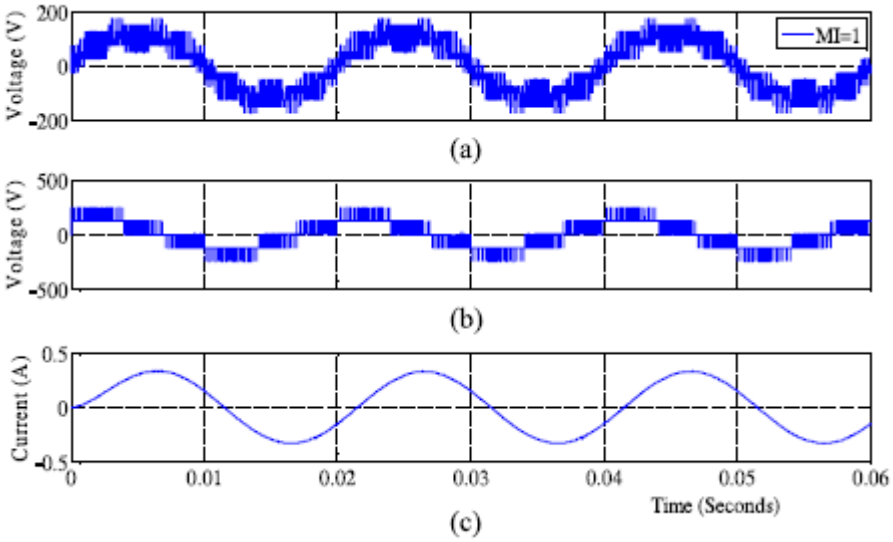

Fig.6 Line and Phase voltage with modulation Index 1

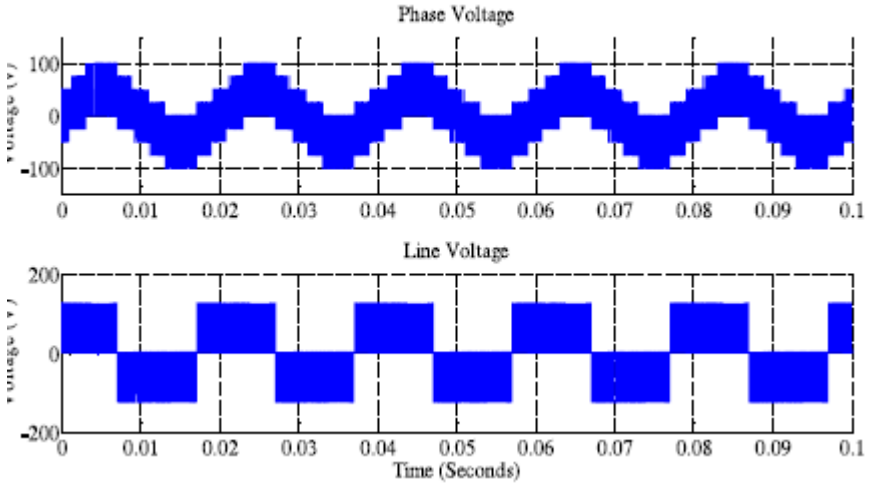

Fig.7 Line and Phase voltage with modulation Index m=0.4

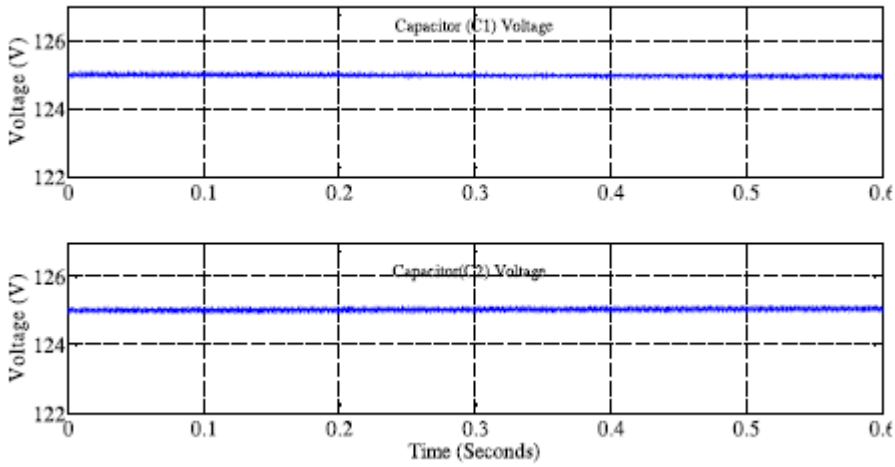

Fig 8. Capactior voltage of C1 and C2

VI. Conclusion

In this paper, a worked on SVPWM is proposed for the threelevel five-stage inverter. The proposed technique doesn't need the fluffy cycle like area distinguishing proof, locale ID specifically area in view of the regulation record, and an ideal changing succession to acquire the abide time. Rather, it utilizes the two-level exchanging time and transporter file to acquire the abide season of ideal five vector exchanging technique. Accordingly, the intricacy in choosing ideal vectors for three-level five-stage is significantly diminished. The proposed technique applies the ideal exchanging succession in view of two-level exchanging state and transporter record. Additionally, the proposed improved on technique uses the excess voltage vectors to adjust the dc-connect capacitor voltage by applying the repetitive vectors time for equivalent time. The variety in dc midpoint voltages of the capacitor is viewed as around 2% tentatively. The transporter record has just to be changed for expansion of this calculation to a staggered inverter having odd number of stages more than three.

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