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Comparative study of Junction-less Field Effect Transistors for Short Channel Effect

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Abstract: -
In this study, we probe the performance of junction less field- effect transistors (JL FETs) with lapping gates in short channel configurations. The lapping gates can significantly reduce the gate- to- channel distance, therefore enhancing the device performance [10]. We perform a relative analysis of two different JL FET designs conventional JL FET and JL FET with lapping gates (OG- JL FET). The simulations are carried out using a marketable TCAD tool to estimate the device characteristics similar as transconductance(gm), subthreshold swing (SS), drain- convinced hedge lowering (DIBL), threshold voltage (Vth), and drain current (Ids) [11].
Keywords: - *Junction less transistor (JLT), Short Channel sequel (SCE), Double- gate MOSFET(DGMOS), gate imbrication.*

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I. INTRODUCTION

With the nonstop scaling of MOSFET bias, the conventional transistor designs are facing multitudinous challenges similar as increased short channel goods, high leakage currents, and difficulty in controlling the channel doping. Junction less field- effect transistors (JL FETs) have surfaced as a promising volition to conventional MOSFETs due to their simpler device structure and process with the conventional CMOS process. In JL FETs, the channel doping is excluded, and the gate electrode controls the channel range by forming a reduction region in the channel. The elimination of the junctions also reduces the junction capacitance and improves the device performance.

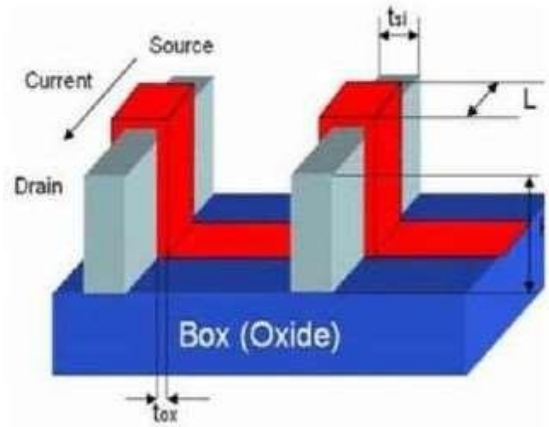


Figure 1- a FinFETs three- dimensional project. H is the stretch and height of the double-gate transistor's fin.

The gate imbrication increases the operative channel extent while dwindling the SCE. The restriction on silicon body consistence tsi is therefore also eased. It's only practicable to achieve the stylish tsi and gate lap Lunn by utilising a fine implicit division model. The logical models

for double-barreled gates that are presently accessible [7], [8] cannot be exercised right down in gate overlap bias due to gate fringing field goods in nonoverlap necks.

The implicit division of a DGMOS transistor with imbrication cannot be determined analytically, as far as we're apprehensive.

The following are the main benefactions of this summary: -
The first system allows for the logical computation of the body eventuality in underlap DGMOS in the subthreshold region (Vgs Vth); the alternate system makes use of the proffered model to determine the combination of Lunn and tsi, which leads to the asked SCE (duct- convinced hedge lowering (DIBL) and subthreshold pitch (SS).
In slim body double-gate bias, punch through current overflows at the locus of SOI bias [9]. To describe the body locus eventuality, we singly break the Poisson equation in the nonoverlap and lap regions with able boundary conditions. In order to reduce computational complication, these short uses a parabolic implicit appraisal in the device body. Due to the fringing field's nonhomogeneous boundary conditions, deciduous- mode dissection doesn't affect in a clear unrestricted- shape result. We performed expansive simulations in the TAURUS device simulator to try our proffered model for colorful shapes and dynamic impulses.

II. Characteristics Properties

Turn–on characteristics and output characteristics*:* -

The 2- D schematic viewpoint of the DG JL FETs is shown off in Figure. also, L stands for the channel extent, and tb and tox sit for the silicon body and gate oxide layers, singly. W indicates that the waterway is wide. For n- type and p- type FETs, singly, ND and NA indicate the steady impurity attention. A JL FET has the same kind and amount of doping in both the S/ D region and the body region. The device has a gate electrode to check it on both the top and bottom. call n- type DG JL FETs as an illustration. We exercise SILVACO TCAD Tools to pretend the DG JL FETs and define each device's tox1.5 nm.

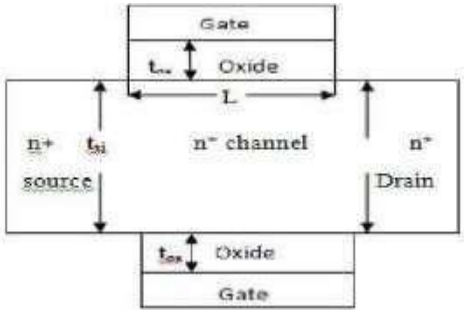


Fig 2. A DGJL FET in 2D schematic standpoint.

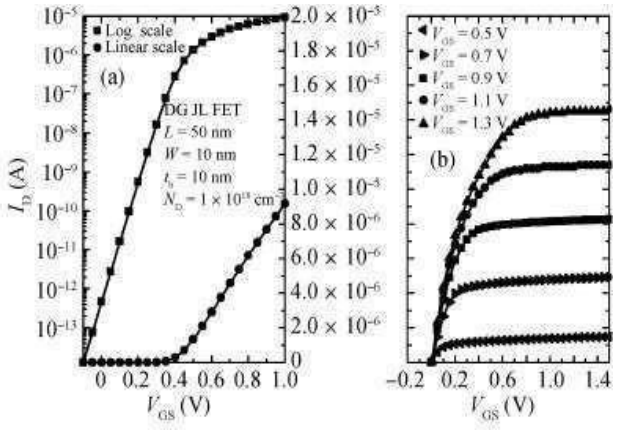


Fig:3(a) and Fig:3(b)

Fig. shows the turn- on characteristics of the DG JL FET with conduit- to- source voltage VDS = 1V. plots the affair characteristics of the same DG JL FET for a gate- to source voltage VGS ranging between0.5 and1.3 V in way of 0.2 V. A comparison of the turn- on characteristics between a DG JL FET and DG IM FETs is shown off in Fig. The JL FET's threshold voltage VT is lower than the IM FET's with the same VDS (VDS = 1 V). The traditional

MOSFETs' threshold voltage is restrained, making it equal to the threshold voltage of DG JL FETs. It can be discerned from the figure that the DG JL FET has a truly analogous property as the DG IM MOSFET. the comparison of the division of electron attention between the two bias above with the same VGS (VGS = 0.2 V) and

VDS (VDS = 0.05 V) in the vertical instruction of the channel at the point of L/ 2. The influence on bias of VDS can be overpassed when VDS = 0.05. JL FETs has a lower electron attention than usual FETs when the same portions apply.
MOSFETs, which explains why in this case the JL FET requires a lower threshold voltage and a lower VGS to switch on.

2.1 Influence of channel length

2.1(a). Impact of channel extent on threshold voltage: -

The comparison of the turn- on features of juncture less and usual bias is shown in above figure. The two orders of bias's body doping are n- type and p- type, and the Both have doping quantities of 2 × 10^18 cm- 3. The VDS contexture is 1 V. As demonstrated, the threshold voltages of the two-bias fall as the channel lengths dock, and the revise in VT for the DG JL MOSFETs is lower than for the DG IM MOSFETs, indicating that DG JL MOSFETs are less affected by the channel extent than DG IM MOSFETs are. The turn- on features of bias with VDS = 0.05 are displayed in above figure. The sequel of the VDS on widgets can also be disregarded. As the channel extent grows shorter, both threshold voltages drop, but it can also be discerned that the DG JL MOSFETs have lower of a jolt on VT.

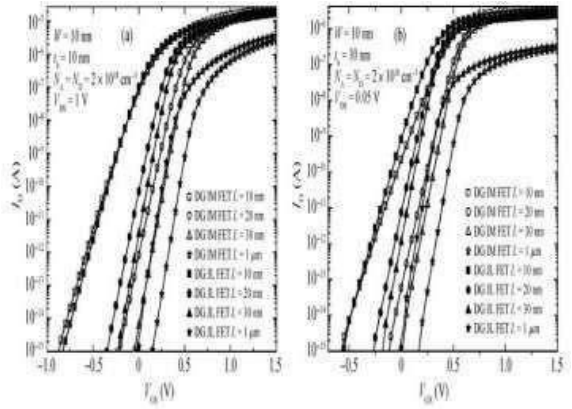


Fig: 4 shown Conventional Devices.

The image makes it easier to understand how changing the channel extent affects both manners of bias's threshold voltages. Indeed, at a lower VDS of 0.05 V, the DG IM MOSFET's threshold voltage changes by around 0.6 V when the channel extent is lowered to 10 nm, but the DG JL MOSFET's threshold voltage changes by around0.43V. Advanced duct- to- source situations have the same outgrowth.

2.2 Influence of channel extent on the subthreshold slope: -

The subthreshold slope (SS), which is measured as the slope of the gate voltage versus the log of the duct current below the threshold(mv/dec), has an impact on the inert current and converting authority operation.

$$SS = \frac{dV_G}{d \lg I_D}.$$

The number taken as the SS represents the subthreshold region's most noble revise. SS is a pivotal physical parameter for measuring how snappily a device transitions from the unacceptable country to the open country and for illustrating how snappily a device opens. A device unlocks more snappily the lower the SS is. We model the SSs of the DGIMFET mentioned over. The impact of SS- L for the two bias is shown in Figure. It's apparent that as L is downgraded, the SS rises. The DG JL FET's jolt on the SS of L, still, is lower than that of the DG IMFET.

2.3 Influence of the doping concentration: -

We will exercise the DGJLFET as an illustration. We also analogize the turn- on parcels of nanowires with colorful doping attention. With the extension of the channel's doping attention, the VT is discerned to dwindle. For the same VGS, advanced doping attention causes an advanced electron attention in the body area. In

other words, in an advanced doping script, there will be more carriers in the channel, making it harder to fully deplete the body area. To achieve nearly no moving electrons in the channel when the doping attention is too high to be fully depleted, we need a further inhospitable voltage. presently, the device's VT is inhospitable. We determine how the threshold voltage VT differs for each of the DG JL MOSFETs' colorful body doping attention, and we also define the wind in figure. With adding channel doping attention, the measure in threshold voltage can be discerned more easily.

Because JL FETs relies on maturity carriers to switch on, the quantum of maturity carriers in the channel increases with device doping attention, lowering the needed VGS for device conduction. As a result, the VT of JLFETs diminishes as the doping attention rises. While nonage carriers are exercised by traditional MOSFETs. The body has a harder time forming the inversion subcaste with an advanced channel doping attention, and the device requires an advanced VGS to turn on. As a result, the threshold voltage of traditional MOSFETs rise along with the attention of channel doping. JL FETs and standard-issue MOSFETs with colorful situations of doping are assimilated in Figure. You can observe the colorful ways in which the threshold voltage changes depending on the quantum of doping in JL FETs and standard-issue MOSFETs.

2.4 Influence of body consistence

The body consistence of the DGJLFET changes from 5 to 20 nm when the L, W, and ND values are set to 20 nm, 10 nm, and 1 × 10^18 cm- 3, independently. The comparison of the simulation findings is shown in Figure. The control area of the gate is the same for all bias because they all have the same channel length and breadth. The number of maturity carriers regulated by the gate varies with changes in body consistence. The further maturity carriers the bias have, the harder it's for the depleted body region to develop in the

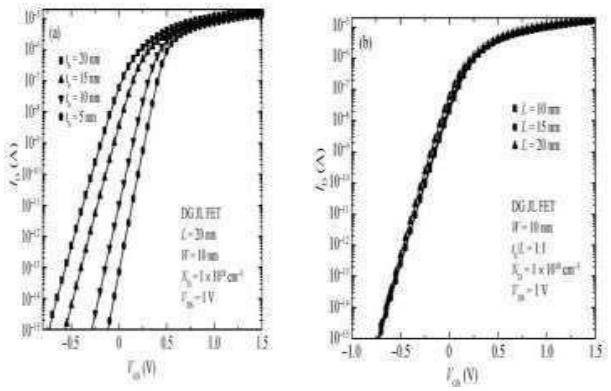


Fig:5 Comparison of the Simulation Findings.

subthreshold region under the same lower gate bias. thus, as body consistence increases, the threshold voltage drops. The SSs of the forenamed four bias are, similarly, 63, 72, 94, and 128 mV/ dec. With an increase in body consistence, SS precipitously rises. In other words, as the body consistence decreases, the junction less case's switching speed from the off state to the open state precipitously increases, as does the capability to regulate gate bias. The three shapes act one another a lot.

2.5 Distributions of electron attention and electrostatic eventuality in the channel direction with different tb: -

Change the three bias's VGS and VDS to 02 V and0.5 V, independently. Fig displays the distribution of electron attention and electrostatic implicit with colorful tb along the channel at a position 1 nm from the face of the silicon body. The electron attention and electric eventuality are shown in above figure, independently. It can be seen that when junction less bias have the same channel length but different tbs, the thicker tb case can contain further maturity carriers in the channel body region, which makes it harder for the gate bias to deplete the channel region in the subthreshold region under the same impulses. The face electron attention for the larger tb case is also lesser, as shown in Figure. In other terms, as shown in Fig, the face eventuality for a larger tb should also be advanced(b). Following that, it can be prognosticated that larger tb cases will beget more subthreshold current for bias with the same impulses and channel length but different tb. This vaticination is harmonious with the simulation results shown in Fig.

2.6 Distribution of electron attention, electric field and the electric eventuality in the vertical channel direction:

Independently, the comparison of the distribution of electron attention, electrostatic eventuality and electric field in the vertical channel direction in different situation. Figure shows the partial blow-up of the electric Field.

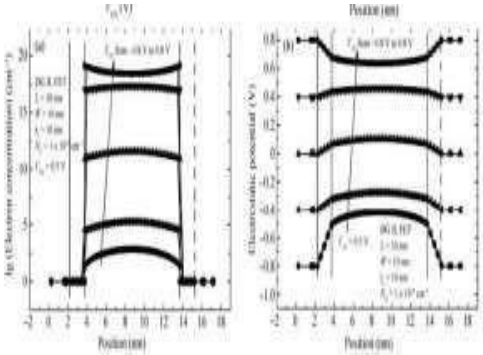


Fig. 6 Distribution of electric field, potential in the perpendicular channel orientation.

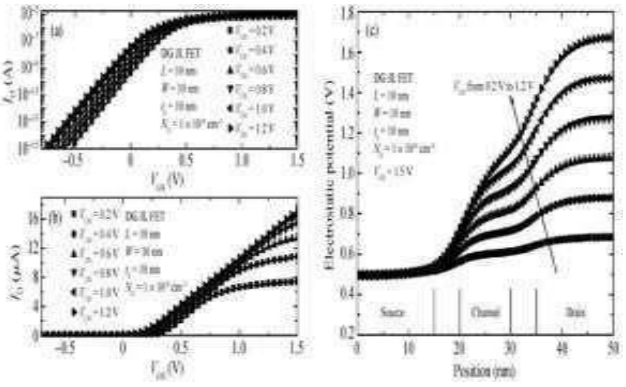
Figure shows how the electric field, eventuality, and attention of electrons are distributed in the vertical channel exposure. Acclimate the gate voltage to2.0 V and set VDS to0.5V. (08, 04, 0,0.4,0.8 V). (A) A comparison of the spread of electron attention in colorful circumstances along the vertical channel direction(b) The electric implicit distribution. (c) The electromagnetic field's distribution. (d) A slight expansion of the electromagnetic field.

The strong electric force causes nearly all of the electrons in the body region to pipe out when the applied gate voltage falls below a certain threshold. The electron attention of the body face and body central region are extremely low, vastly lower than the doping attention of silicon nanowire. It implies that the entire body region can be considered to be roughly fully depleted. Because the face of the body has the topmost position of VGS control, there are smaller electrons there than in the central region. As VGS increases, the reduction precipitously disappears until it approaches the flat band value. The source and drain are connected when the applied gate voltage exceeds the device threshold voltage and a specific number of electrons have accumulated in the channel region.

Also, due to these variations, the implicit wind's curve gradationally decreases to zero while the face and the central area return to their original positions. The channel eventuality also keeps rising as the gate voltage rises, which causes electrons to gather on the face of the body area. also, compared to the central area, the electron attention is advanced near the face region.

2.7 Influence of drain voltage:

Set the DG JL FET's parameters. numbers 7(a) and 7(b) plot the turn- on characteristics in log and direct scales of the DG JL FET for different VDS, independently.



Above figures shows the DG JL FET's turn- on features in log form for colorful VDS(V). Linear scales of turn- on features. Electrostatic implicit distribution of the DG JL FET in the channel direction for VDS ranging from0.2 to1.2 V in way of 0.2 V and VDS = 1.5 V at the position of tb/ 2.

The distribution of electrostatic eventuality at the L/ 2 position along the vertical channel direction with rising VDS, the electrical eventuality rises as well. The two widgets' SS- VDS angles. With the rise in VDS, SSs of both types of bias rise. DG JL FET of VDS's effect over SS is less significant than it's for DG IM FET. It's apparent that as VDS increases, the threshold voltage diminishes. The spread of is shown in Figure. Electrostatic eventuality for VDS varying from 0.2 to1.2

V in way of0.2 V and1.5 V at the point of tb/ 2 in the channel direction of the DG JL FET. The spread of electrostatic eventuality along the channel's vertical direction at L/ 2 is depicted in Figure. In the two plots, the electrostatic eventuality rises as VDS rises. For the six VDS values, pretend the SSs of the DG JL FET described over and the DG IM FET using the same settings. The SS- VDS line for each of the two bias is shown in Figure. With the rise in VDS, SSs of both types of bias rise. still, DG JL FET's impact on SS of VDS is lower than DG IM FET's, indicating that JL FETs is more stable in this regard. All the characteristics of traditional DG MOSFETs are present in DG JL FETs. This study examined the goods of channel length, body consistence, and doping attention on the threshold voltages and subthreshold pitch of short- channel JL FETs. JL FETs is less affected by channel length and VDS under the same circumstances than standard FETs are.
Because of these benefits, the JL FET can be a wise option for SCEs.

III. Method:

The simulations are carried out using a marketable TCAD tool (Silvaco Atlas) with the following specifications Si (100) substrate with a consistence of 400 nm, gate oxide consistence of1.5 nm, gate length of 20 nm, and gate work function of4.2 eV. We pretend two different JL FET designs conventional JL FET and JL FET with lapping gates (OG- JL FET). The imbrication length is varied from 5 nm to 15 nm to probe the effect of lapping gates on device performance.

IV. Simulation Results:

The OG- JL FET shows an advanced transconductance(gm) and drain current (Ids) compared to the conventional JL FET. The gm of the OG- JL FET is1.76 mS/ μm, which is 12 advanced than the conventional JL FET. also, the Ids of the OG- JL FET is 562 μA/ μm, which is 8 advanced than the conventional JL FET.

The subthreshold swing (SS) of the OG- JL FET is also lower than the conventional JL FET. still, the OG- JL FET shows an advanced drain- convinced hedge lowering (DIBL) and threshold voltage (Vth) compared to the conventional JL FET.

V. Conclusion:

In conclusion, the JL FET with lapping gates (OG- JL FET) shows advanced device performance compared to the conventional JL FET. The lapping gates reduce the gate- to- channel distance and enhance the device characteristics similar as transconductance(gm) and drain current (Ids). still, the OG- JL FET also shows advanced DIBL and Vth compared to the conventional JL FET, which can be eased by optimizing the device design parameters. Overall, the proposed OG- JL FET design can give a promising volition for short- channel bias with bettered performance.

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