International Journal of Research in Engineering and Science (IJRES)
ISSN (Online): 2320-9364, ISSN (Print): 2320-9356
www.ijres.org Volume 11 Issue 10 ǁ October 2023 ǁ PP. 465-468

Nanotechology Based on A New Complete Cell of Agricultural Quaternary

Er. Rohit Kumar* Er. Maheswar Mallick**, Er. Prativa Manjari Barik***
** Department Of Civil Engineering, Swami Vivekananda School of Engineering & Technology, Madanpur, Bhubaneswar, Odisha-752054*
***Department Of Civil Engineering, Swami Vivekananda School of Engineering & Technology, Madanpur, Bhubaneswar, Odisha-752054*
****Department Of Civil Engineering, Swami Vivekananda School of Engineering & Technology, Madanpur, Bhubaneswar, Odisha-752054*

ABSTRACT:-
Binary logic circuits are limited by the requirement of interconnections. A feasible solution is to transmit more information through a signal line and using multiple value logic (MVL). This article presents a new high-performance quaternary complete adder cell based on a carbon nanotube field effect transistor (CNTFET). The proposed quaternary full adder is designed in multiple value voltage mode. CNTFET is a promising candidate to replace MOSFET with some useful properties, such as the ability to have the desired threshold voltage by regulating the nanotube diameters, which makes them very appropriate for the design of multi-threshold circuits in voltage mode. The proposed circuit is examined, using Synopsys HSPICE with the standard 32 nm CNTFET technology with different temperatures and supply voltages.

KEYWORDS:- *Carbon nanotube FET (CNTFET), Quaternary logic, Full Adder, Multiple-5th design, Nano-electronics.*

I. INTRODUCTION:-

Traditional computer systems use binary logic for their operations. However, multiple value logic (MVL) circuits have been designed in recent decades as an alternative to binary circuits. The main advantage of MVL is the reduction in the number of interconnections, which is a serious problem in today's binary integrated circuits. The multi-value logic seeks to improve the efficiency of the information processing of a circuit by transmitting more information in each signal line than simple binary logic and implementing complex functions of the inputs in a single door. However, the use of MVL has been restricted due to the fact that compact and stable MVL circuits are difficult to design, noise margins on multiple rated lines are reduced and most importantly it is necessary to convert to and from the binary world. Accordingly, designers using the MVL paradigm have mostly focused on the ternary (i.e. radix 3) and the quaternary (i.e. radix-4) number systems. Ternary system consists of three digits, namely {0, 1, 2} and quaternary system consists of four digits {0, 1, 2, 3}. However, quaternary logic seems to be more interesting due to the simple conversion between quaternary signals and binary signals. On the other hand, scaling down the feature size of the metal-oxide semiconductor (MOS) technology deeper in nano-ranges leads to numerous critical challenges and problems, which will considerably reduce its suitability for energy efficient applications in the time to come. To overcome these problems, such as short channel effects, reduced gate control and high leakage power dissipation, researchers are working towards new technologies. These technologies, such as single electron transistor, quantum dot cellular automata and carbon nanotube field effect transistor (CNTFET) are being studied to replace the customary silicon based CMOS technology in the near future [1]-[3]. Among these emerging nanotechnologies, CNTFET seems to be more appropriate on account of its likeness with MOSFET in terms of inherent electrical properties which makes it possible to utilize previously designed CMOS structures in the CNTFET technology without any significant modifications. Moreover, the unique one-dimensional band structure of the CNTFET represses backscattering and causes near-ballistic operation, which results in very high-speed operation [4]. One of the important properties of CNTFETs which is very useful for transistor sizing of complex circuits is the same mobility for N-FET and P-FET and consequently same current drive capability. Generally CNTFETs are faster than MOSFETs and also consume less power. MVL circuits can be designed either in current mode or voltage mode. CMOS voltage mode MVL circuits are based on multiple-threshold design which can be achieved by applying different bias voltages to the bulk terminal of transistors. This method is not efficient and leads to very complex and high-cost fabrication. In a CNTFET, the threshold voltage of the transistor is determined by the diameter of the CNT. Since, a multiple threshold design can be carried out by adopting CNTs with different diameters for different CNTFETs. Accordingly, proposing new efficient CNFET-based designs for quaternary logic is of an interest. In this paper we proposed an efficient

quaternary full adder cell based on carbon nanotube field effect transistor. Full adder cell is one of the most important ingredients in a processing system and designing a high-performance Full adder cell would increase the performance of whole system [5].The organization of the rest of the paper is as follows: section 2 reviews the carbon nanotube field effect transistor. The proposed CNFET-based quaternary Full adder is described in section 3. In section 4 the simulation results are presented and finally the paper is concluded in section 5.

II. CARBON NANOTUBE FIELD EFFECT TRANSISTORS (CNFETS):-

The carbon nanotube is considered fundamentally as a graphite sheet rolled in a tube with a diameter of few nanometers and a length of up to several micro meters. CNTs are classified as single wall CNT (SWCNT), composed of a single cylinder and multi-wall CNT (MWCNTs), consisting of more than one cylinder [6]. The the way the graphite sheet is rolled is represented by a pair of indexes called chiral numbers. These indices indicate the Z) is∈conductivity of a CNT. A CNT with n-m = 3k (k metal; otherwise it is a semiconductor that can be used as the channel of a CNFET. CNT is the most promising candidate to create. Transistors on a smaller scale than silicon transistors due to its excellent electrical properties, such as quasi-logistics carrier transport and short channel suppression effects due to the one-dimensional transport of electrons. In addition, a CNTFET has similar I-V characteristics with a well tempered MOSFET but with a considerable smallest channel length modulation parameter [7]. Figure 1 shows a typical CNTFET device. Distance between the centers of two adjacent CNTs below the The same door of a CNTFET is called Pitch, which has a direct impact on the width of the contacts and the door of the transistor.

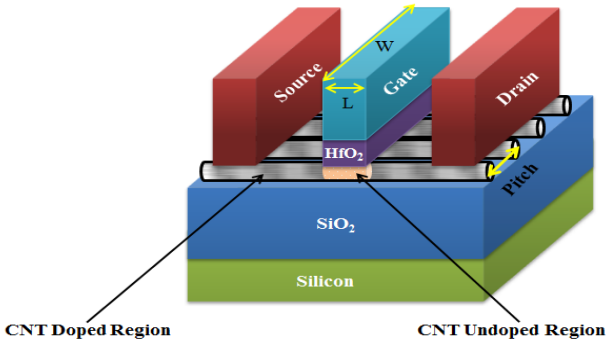

Fig 1. MOSFET-like CNTFET Device

This feature of CNTFETs indicates that by changing the CNTFETs diameters can easily acquire different transistors with different turn on voltages. This practical characteristic makes CNTFET very appropriate for designing voltage-mode MVL circuits. Where, a(≈0.249 nm) is the carbon to carbon atom distance, Vπ (≈3.033 eV) is the carbon π–π bond energy in the tight bonding model and DCNT is the diameter of the nanotubes. Different types of CNTFETs have been presented so far [9]. One of them is Schottky Barrier CNTEF (SB-CNTFET). SB-CNTFET has direct contact between the semiconducting CNT and the metal; hence Schottky Barrier exists at the metal nanotube junction. In this type of CNTFETs by changing the barrier height at the metal semiconductor interface, gate modulates the injection of carriers in the nanotube. Due to exhibition of strong ambipolar characteristics, SB-CNTFETs are not suitable for using in CMOS logic families. Another type of CNTFETs is MOSFET-like CNTFET (MOS-CNTFET) which exhibit unipolar behavior unlike SB-CNTFET. In this MOSFET like device, the ungated portions (source and drain regions) are heavily doped and the CNTFET operates on the principle of barrier height modulation by application of the gate potential. The conductivity of MOS-CNTFET is modulated by the gate-source bias. Both SB-CNFETs and MOS-CNFETs are used for high speed design because of their high ON current. However, the other type of CNTFET, band-to-band tunneling CNTFET (T-CNTFET) is utilized for ultra-low-power design on account of its low ON current and supper cut-off attributes.

III. PROPOSED QUATERNARY FULL ADDER CELL:-

Quaternary logic includes four significant logic levels which can be demonstrated by ―0‖, ―1‖, ―2‖ and ―3‖ symbols. These logic levels are commonly equivalent to 0 V, 1/3VDD, 2/3VDD and VDD voltage levels, respectively. In this work, we propose a new quaternary full adder cell based on Carbon nanotube field effect transistors. Quaternary full adder has three inputs (A, B, C) and two outputs (Sum, Cout) which can take values of 0,1,2,3. Although the concept of multiple valued logic has existed for a long time, but there are rare efforts on designing quaternary full adder. Nearly all quaternary full adder circuits which have been proposed so far have been designed based on multiple supply voltage and assumed that *carry in* is 0 or 1 [10]-[12], which is an unrealistic simplification. However, in this paper we propose a quaternary full adder which has a single supply voltage and assume that *carry in* can take all four possible values (0, 1, 2, 3).

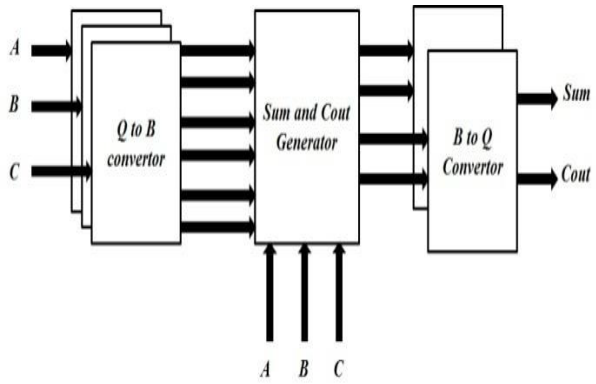

Fig 2. The proposed quaternary full adder (CQFA)

IV. SIMULATION RESULTS:-

In this section simulation results of the proposed quaternary full adder are presented. The Synopsys HSPICE simulator with the compact SPICE model for CNTFETs is used for the simulations at 32nm technology node [14]-[16]. This model is designed for unipolar MOSFET-like CNTFET devices and each transistor can have one or more CNTs under its gate. Simulations are conducted at 0.9V and 1V power supplies, at different temperatures and with different load capacitors. The delay of each circuit is calculated from the time that the input signal reaches the half of its voltage level to the time that the output signal reaches the half of its voltage level. The average power consumption is also considered as the power consumption parameter. The transient response of the proposed design is demonstrated in Fig 8. It shows the correct operation of the proposed quaternary full adder. Figures 3, 4 and 5 show the delay, power consumption and PDP of the proposed quaternary full adder with different load capacitors. Also fig 6 shows the PDP variations of the proposed quaternary adder against temperature variations.

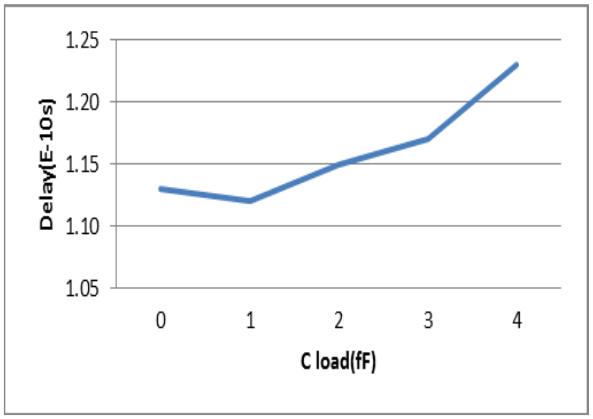

Fig-3-Delay of the proposed circuit versus load capacitance variation

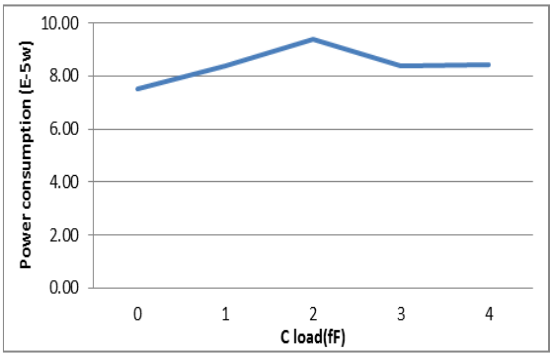

Fig-4-Power of the proposed circuit versus load capacitance variation

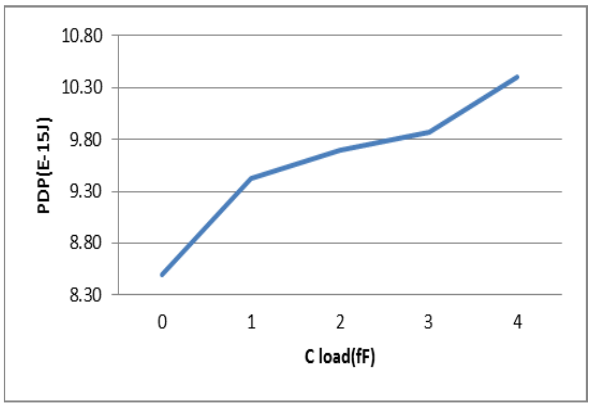

Fig-5-PDP of the proposed circuit versus load capacitance variation

V. CONCLUSION:-

In this article, a high performance CNTFET based quaternary full adder cell has been proposed. As the threshold voltage of the CNTFET is related to the geometry of the CNTFET (DCNT), a new multi-diameter and consequently multi-threshold voltage CNTFET based quaternary full adder design has been introduced in this paper. Proposed quaternary full adder is designed with quaternary to binary converter, sum and carry generator and binary to quaternary converter. All simulations have been performed in HSPICE using the CNTFET model at 32nm technology node.

REFERENCES:-

[1]. A. Raychowdhury and K. Roy,"Carbon nanotube electronics: design of high-performanceand low-power digital circuits",Circuits and Systems I: Regular Papers, IEEE Transactions on, Vol. 54, No. 11, pp. 2391-2401, 2007.
[2]. S. Sayedsalehi, M. H. Moaiyeri and K. Navi,"Novel Efficient Adder Circuits for Quantum-Dot Cellular Automata", Journal of Computational and Theoretical Nanoscience, Vol. 8, No. 9, pp. 1769-1775, 2011.
[3]. M. H. Moaiyeri, A. Doostaregan and K. Navi,"Design of Energy-Efficient and Robust Ternary Circuits for Nanotechnology", IET Circuits, Devices & Systems, Vol. 5, No. 4, pp. 285–296, 2011.
[4]. S. Lin , Y. B. Kim and F. Lombardi,"CNTFET-based design of ternary logic gates and arithmetic circuits",Nanotechnology, IEEE Transactions on, Vol. 10, No. 2, pp. 217-225, 2011.
[5]. K. Navi, M. H. Moaiyeri, R. Faghih Mirzaee, O. Hashemipour, and B. Mazloom Nezhad,"Two new low-power full adders based on majority-not gates", Elsevier, Microelectronics Journal, Vol. 40, No. 1, pp. 126-130, 2009.
[6]. McEuen, P. L. Fuhrer, M. Park,"Single-Walled Carbon Nanotube Electronics", IEEE Transactions on Nanotechnology. pp. 78-85, 2002.
[7]. R. Zarhoun, M. H. Moaiyeri, S. S. Farahani and K. Navi, "AnEfficient 5-Input Exclusive-OR Circuit Based on Carbon Nanotube FETs",ETRI Journal, Vol. 36, No. 1, pp. 89-98, 2014.
[8]. Y. B. Kim, F. Lombardi,"Novel design methodology to optimize the speed and power of the CNTFET circuits", Proc IEEE International Midwest Symposium on Circuits and Systems, pp.1130-1133, 2009.
[9]. Raychowdhury, K. Roy,"Carbon nanotube electronics: design of high-performance and low-power digital circuits", IEEE Transactions on Circuits andSystems. 54(11). pp. 2391-2401, 2007.
[10]. K. Vasundara Patel S, K. S Gurumurthy,"Design of High Performance Quaternary Adders", International Journal of Computer Theory and Engineering, Vol.2, No.6, 2010.
[11]. I.M. Thoidis, D. Soudris, J. M.Fernandezl and A. Thanailakis,"THE CIRCUIT DESIGN OF MULTIPLE-VALUED LOGIC VOLTAGE-MODE ADDERS", IEEE International Symposium on Circuits and Systems,2001.
[12]. H. Shirahama, T. Hanyu,"Design of High-Performance Quaternary Adders Based on Output-Generator Sharing", 38th International Symposium on Multiple Valued Logic, 10.1109/ISMVL, 2008.
[13]. M. H. Moaiyeri, K. Navi and O. Hashemipour,"Design and Evaluation of CNFET-based Quaternary Circuits", Springer, Circuits, Systems, and Signal Processing, Vol. 31, No. 5, pp. 1631–1652, 2012.
[14]. J. Deng, H-S.P. Wong,"Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region", IEEE Transactions on Electron Device. 54, (12). pp. 3186-3194, 2007.
[15]. J. Deng, Wong,"A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking". IEEE Transactions on Electron Device. 54 (12). pp. 3195-3205, 2007.
[16]. J. Deng,"Device modeling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45 nm node and carbon nanotube field effect transistors," Doctoral D