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Design of Low Voltage Low Power Voltage Differencing Dual X current conveyor in 0.18µm CMOS Technology

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Abstract
Advancement in VLSI technology has led to largernumber of components on a single chip making it a reality to realizeportable systems. Analog circuits are important in every VLSI systemsuch as filters, current and voltage amplifiers, comparators, A/D andD/A converters, etc. Miniaturization in circuit design requires lowpower low-voltage (LPLV) analog integrated circuits to be designed.Analog signal processing's inherent advantage of low power and highspeed has led to extensive research in analog domain. Current domainprocessing having advantages of higher bandwidth, large dynamicrange, greater linearity, simple circuitry seems to be the solution.Among the number of current mode topologies current conveyor is themost versatile building block. In this research floating gate technique is used in the design a versatile current mode active block the voltage differencing dual x current conveyor (VD-DXCC). The VD-DXCC is designed using 0.18µm technology in Spice software for a supply voltage of ±0.9V. Number of simulation analysis are done to validate the design.

Keywords: *Analog circuits, Current mode, Current conveyor, Signal processing*

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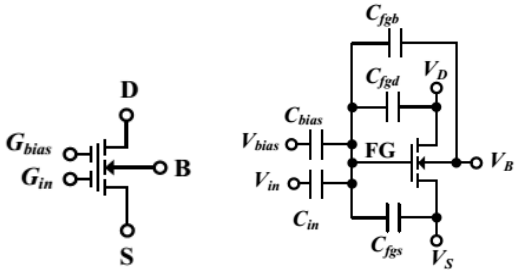
I. INTRODUCTION

With scaling down of CMOS to comply with large scaleintegration and system on chip requirements together withincreased demand for portable and battery-operated devices, lowpower low voltage (LP LV) devices are need of the hour. Thecurrent mode devices are more suited for (LP LV) operation thantheir voltage counterpart [1, 2]. Current mode circuits are moreimmune to noise, less sensitive to supply voltage and have lowelectrostatic discharge, low propagation delay, high slew rate etc.[2,4]. Among various current mode devices current conveyor(CC) is the most functional device by virtue of its versatilefeatures such as simplicity in design, higher gain bandwidthproduct, linearity, high frequency operation, less chip area, lowpower dissipation [4-7] etc. In 1968 [1] the current conveyor(CC) was introduced and has since found recognition in bothconceptual and practical implementation. Research publishedin last few years reveals that analog circuit designers are nowconsidering the CC as a building block for designing multitude ofapplications like signal processing, amplification,instrumentation etc. [1,8,9]. A CC is a three-terminal devicehaving a low impedance input, a high impedance inputsimultaneously with a characteristic of virtual short and a highimpedance output terminal [1,3]. Since its introduction manytopologies of CC have been developed, but second generation. current controlled current conveyor (CCCII) gathers largerattention from designers due to its high tunability [1,2,10].CCCII has in built parasitic resistance, which is self-adjustable bybias current, due to this parasitic resistance the requirement ofexternal resistance is reduced. Practical CC has various nonidealities and some of them prove their importance in differentapplications [11, 12]. Parasitic resistance of CCCII is one of itsuseful non idealities. Literature shows there are many tunablecircuits i.e. current conveyor transconductance amplifier(CCTA) [16], current follower transconductance amplifier(CFTA) [17], current controlled current conveyortransconductance amplifier (CCCCTA) [6]etc.

The advancement in miniaturized circuits that can perform specialized tasks like portable activity monitors, smart watches, electrocardiogram (ECG) machines, smart phones and blood pressure monitors etc. The requirement to prolong the battery life span of the devices has increased. These smart battery-operated devices pose four major challenges for the designers. First, longer battery life span, low voltage operation, higher transistor packing density and high operational speed. Since it is not possible to achieve each of the above requirements independently a good tradeoff between the parameters need to be achieved. To achieve performance enhancement and ultra-high packing density aggressiveComplementary Metal Oxide Semiconductor (CMOS) scaling is done. This led to rapid shrink in size of the semiconductor devices, high speed, reduction in supply voltage and reduced power dissipation. This scaling proved beneficial for the digital designs but resulted in severe performance degradation for analog design. The major reason for this is that the

threshold voltage cannot be scaled in the same ratio as the supply voltage and so it takes up a substantial fraction of the total supply voltage leading to decreased dynamic range and bandwidth. To mitigate this problem novel techniques have been developed which can be categorized in two main levels. First, circuit level design technique which includes adopting numerous circuit level techniques to achieve high performance designs like folded cascode, class AB stage, level shifting, subthreshold operation, self cascode and composite transistor. Recently, researchers also utilized special connection of metal oxide semiconductor (MOS) transistor to remove or reduce threshold voltage from signal[18-19]. These include floating gate MOS (FG-MOS), bulk driven MOS (BD-MOS) and dynamic threshold MOS (DTMOS) techniques [18-19]. The FGMOS technique involves leaving the gate electrode floating; two or more control gates are formed over this electrode using a second polysilicon layer deposition. Figure 2.3 (a) presents the symbol of a two-input NMOS Floating-Gate transistor. The equivalent circuit is shown in Figure 2.3 (b). The voltage at the floating gate is given by Equation 2.1.



(a) (b)

Figure 1:(a) The symbol of FG-MOS (b) Equivalent circuit of FG-MOS

$$V_{FG} = \frac{C_{in}V_{in}+C_{bias}V_{bias}+C_{GD}V_D+C_{GS}V_S+C_{GB}V_B+Q_{FG}}{C_{Total}} \quad (1)$$

Where Q_{FG} is the residual charge trapped at the FGMOS during the fabrication process. The total capacitance $C_{Total} = C_{in} + C_{bias} + C_{GD} + C_{GS}+C_{GB}$, where C_{GD}, C_{GS}, C_{GB} are the parasitic capacitances associated with the source, drain and bulk region respectively. If the input capacitance is selected such that their sum is much greater than the parasitic capacitances, then voltage on floating gate is given by Equation 2.2.

$$V_{FG} \approx K_1V_{in} + K_2V_{bias} \quad (2)$$

Where $K_1 = \frac{C_{in}}{C_{Total}}$ and $K_2 = \frac{C_{bias}}{C_{Total}}$ are the equivalent weights. The equivalent threshold voltage of FG-MOS is given by Equation 2.3.

$$V_{Threshold-FG} = \frac{V_T - V_{bias}K_2}{K_1} \quad (3)$$

Where V_T is the threshold voltage of a conventional gate driven MOS (GD-MOS) transistor. It can be deduced from the equation that by suitable choice of K_1, K_2 and V_{bias} the threshold voltage of the FG-MOS can be reduced or made zero.

II. Voltage Differencing Dual X Current Conveyor (VD-DXCC)

The Voltage Differencing Dual X Current Conveyor (VD-DXCC) [20] is functionally a connection of DXCCII and OTA. The new block carries features of inverting current conveyor (ICCII), CCII, and tunable trans-conductor in one single architecture which is also simple to implement and develop into integrated circuit. The Voltage current characteristics of the developed VD-DXCC are given in matrix Equation 4 and the block diagram is presented in Figure. 2.

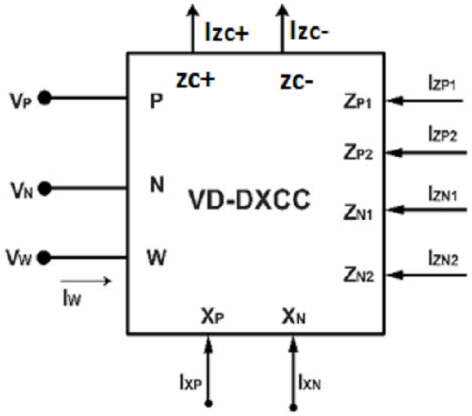


Figure 2: Block diagram of VD-DXCC

$$\begin{bmatrix} I_N \\ I_P \\ I_{zc\pm/I_W} \\ V_{XP} \\ V_{XN} \\ I_{ZP1} \\ I_{ZP2} \\ I_{ZN1} \\ I_{ZN2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_W \\ I_{XP} \\ I_{XN} \\ V_{ZP1} \\ V_{ZP2} \\ V_{ZN1} \\ V_{ZN2} \end{bmatrix} \quad (4)$$

The CMOS implementation of VD-DXCC is presented in Figure 3. It is aneight-terminal active element. The second stage consists of DXCCII, transistors (M13-M32). The voltage at W appears at V_{XP} and in inverted format atV_{XN}. The current input at X_p node is transferred to nodes Z_{P1}andZ_{P2}. In the same way the current from X_N node is transferred to $Z_{N1}$and Z_{N2}. The W and Z nodes are high impedance while the X_P and X_N node are low impedance.The First stage is composed of OTA. The transconductance is realized using transistors (M1-M2). The output current of the trans-conductor depends on the voltage difference between voltages at terminals P and N. Assuming saturation region operation for all transistors and equal W/L ratio for transistors M1 and M2 the output current $I_{ZC+}, I_{\boldsymbol{ZC-}}$ of the OTA is given by Equation 5.

$$I_{\boldsymbol{ZC+}} = -I_{\boldsymbol{ZC-}} = g_m(V_P - V_N) = \left(\sqrt{2I_{Bias}\,k}\right)(V_P - V_N) \quad (5)$$

Where, the transconductance parameter $K_i = \mu C_{ox} {}^{W}/_{2L}$ $(i = 1, 2)$, W is the effective channel width, L is the effective length of the channel, C_{ox} is the gate oxide capacitance per unit area and μ is the carrier mobility. It is evident from (4) that the transconductance can be tuned by the bias current thus imparting tunability to the structure.

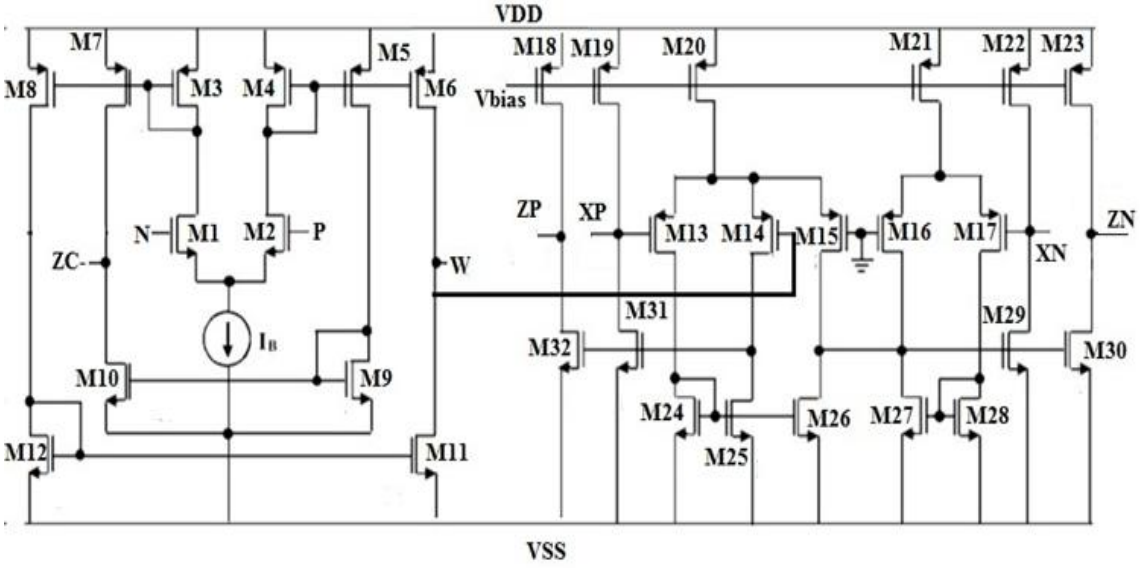


Figure Error! No text of specified style in document.**:CMOS Implementation of VD-DXCC**

III. Non-Ideal Analysis of VD-DXCC

Inthis section the non-idealities of the VD-DXCC are considered and their influence on the proposed filter circuits is analyzed. The frequency dependent non-ideal voltage (β), current (α) andtransconductance transfer (γ/γ') gains cause a slight change in the current and voltage signals during transfer leading to undesired response. Considering the effect of frequency dependent current and voltage transfer gains the V-I characteristics of VD-DXCC are modified as given below in Equations 6-11.

$$I_{ZP} = I_{ZP} = \alpha_P I_{XP} \tag{6}$$

$$I_{ZN} = I_{ZN} = \alpha_N I_{NP} \tag{7}$$

$$V_{XN} = -\beta_N V_W \tag{8}$$

$$V_{XP} = \beta_P V_W \tag{9}$$

$$I_{ZC+} = I_W = \gamma g_m (V_P - V_N) \tag{10}$$

$$I_{ZC-} = -\gamma^{'} g_m (V_P - V_N) \tag{11}$$

Where α is the current transfer gain, β stands for voltage transfer gain and γ denotes the transconductance transfer gain. Ideally their values should be unity.

IV. RESULT AND DISCUSSION

To validate its functionality the VD-DXCC is designed in 0.18µm technology using Spice software at a supply voltage of ±0.9 V. The width and length of the transistors used are given in Table 1. The bias current of the OTA is fixed at 80µA resulting in transconductance of 756µS.

Table 1:Width and Length of the MOS transistors

Transistors	Width (µm)	Length (µm)
M1-M2, M5-M6	2.8	0.36
M3-M4, M7-M9	5.8	0.36
M10-M14	1.8	0.72
M15-M18	.06	0.36
M19-M22	4	0.36
M23, M25, M27, M33, M42, M44	2.16	0.36

4.1 DC Analysis

The DC analysis is carried out to estimate the dynamic range, accuracy and linearity of the current follower, transconductance transfer and voltage follower sections of the proposed VD-DXCC. At first, the voltage follower stage is tested. A dc sweep of ±1V is applied at the W terminal and the output voltage at the X_P and X_N terminals is measured as presented in Figure 4. The dynamic range of the voltage follower stage for W to X_P is ±650mV and W to X_N is ±350mV. The range is calculated by doing error analysis between input and output in the cadence simulator. Secondly, dc sweep of ±100µA is done at the X_P and X_N terminals and the output current flowing in the Z_{P+} and Z_{N+} nodes is measured as shown in Figure 5. The linear current range is found to be I_{ZP+}=±40µA and I_{ZN+}=±40µA beyond this range the error between input and output exceeds 2%. Lastly, the OTA analysis reveals that the linear range of the OTA is approximately ±120µA as presented in Figure 6. Outside this range the output current flowing through the Z_{P+} and Z_{Z+} nodes saturate.

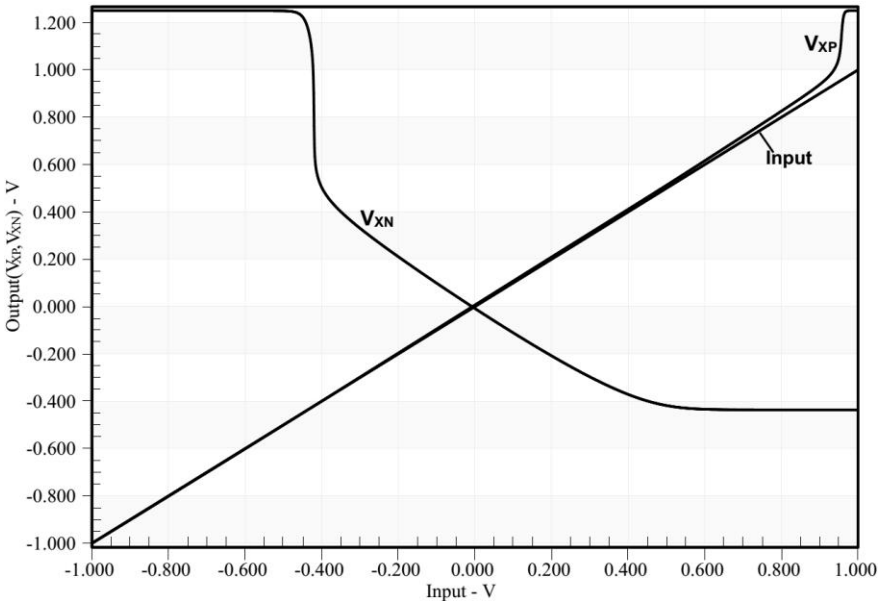


Figure Error! No text of specified style in document.**: DC analysis of the voltage follower**

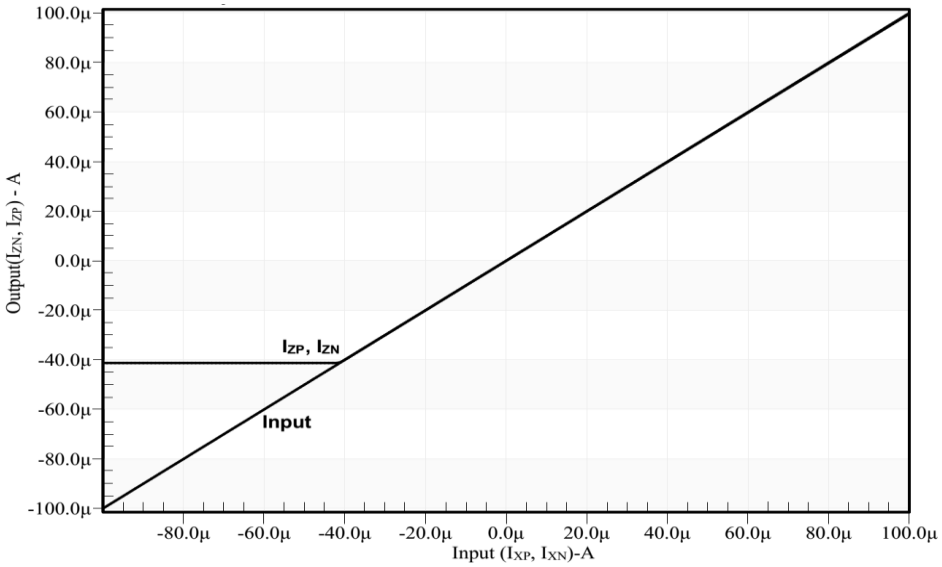


Figure 5: DC analysis of the current follower

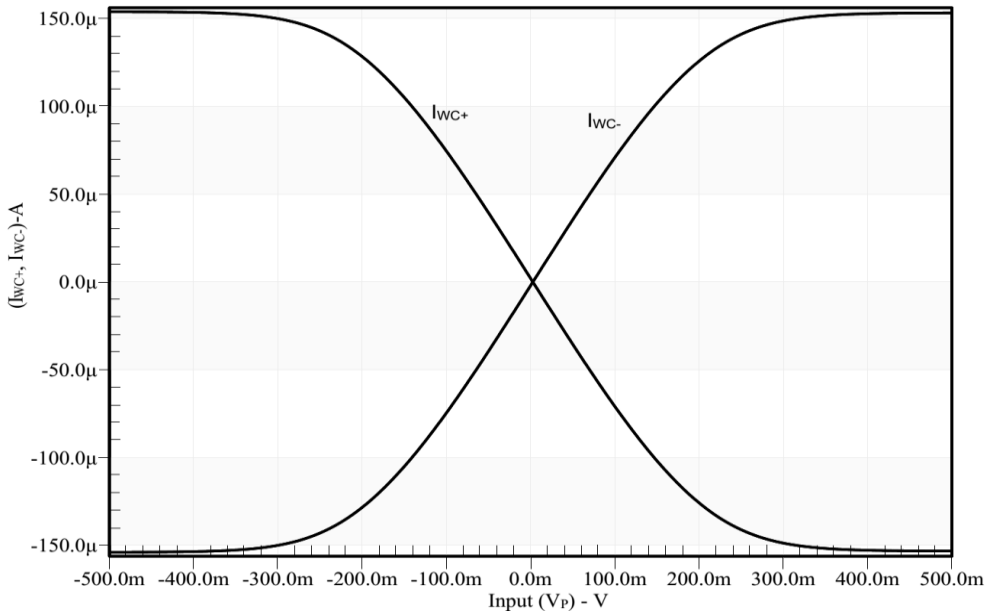


Figure 6: DC analysis of the OTA

4.2 AC Analysis

The ac analysis is conducted to measure the important circuit parameters including bandwidth, current and voltage transfer ratio and various node impedances of the current and voltage follower stages of the VD-DXCC. The transconductance and transconductance transfer bandwidth of the OTA section are also evaluated.

The voltage transfer ratios $\left(\frac{V_{XP}}{V_W}\right)$ and $\left(\frac{V_{XN}}{V_W}\right)$ are measured using AC analysis as presented in Figure 4.19. The ratios are found to be 1.05 and 1.03. The -3dB bandwidth for $\left(\frac{V_{XP}}{V_W}\right)$ is 2.22 GHz and for $\left(\frac{V_{XN}}{V_W}\right)$ is 2.34 GHz. AC analysis of the current transfer stage is conducted and ratios $\left(\frac{I_{ZP+}}{I_{XP}}\right)$ and $\left(\frac{I_{ZN+}}{I_{XN}}\right)$ are measured. The ratios are found to be 1.03 and 0.996 respectively. The -3dB bandwidth for $\left(\frac{I_{ZP+}}{I_{XP}}\right)$ is found to be 2.1 GHz and

for $\left(\frac{I_{ZN+}}{I_{XN}}\right)$ is found to be 2.9 GHz. The analysis plots are presented in Figures 7-9. The transconductance of the OTA is also evaluated and found equal to 756µS as given in Figure 10.

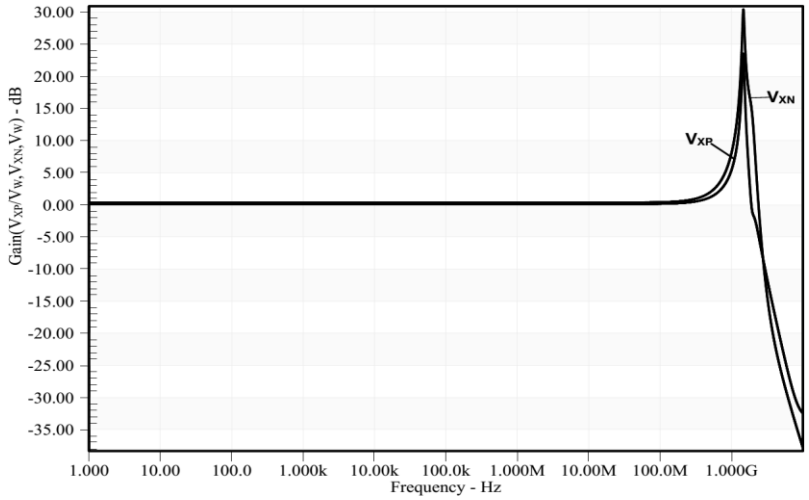


Figure 7: AC analysis of the voltage follower (X_P /V_W,X_N /V_W)

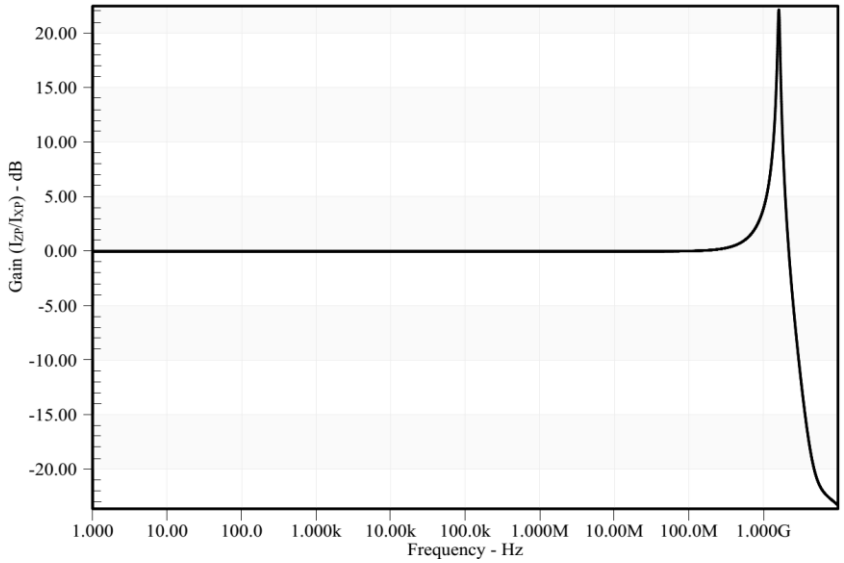


Figure 8: AC analysis of the current follower (I_{ZP}/I_{XP})

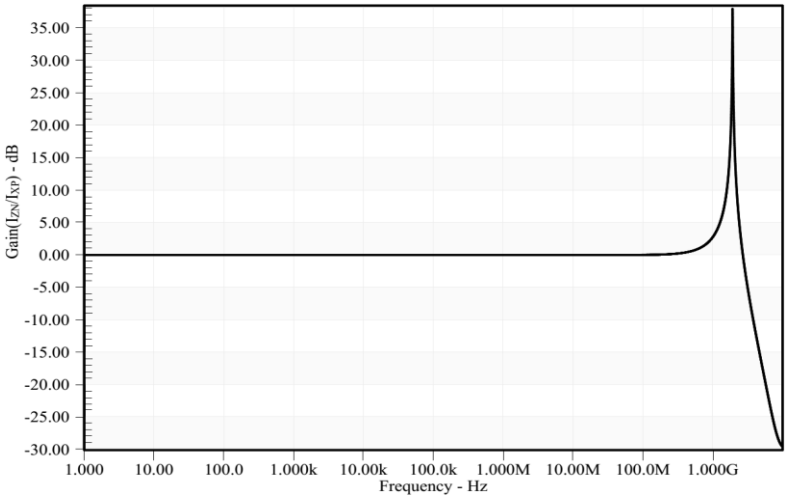


Figure 9: AC analysis of the current follower (I_{ZN}/I_{XN})

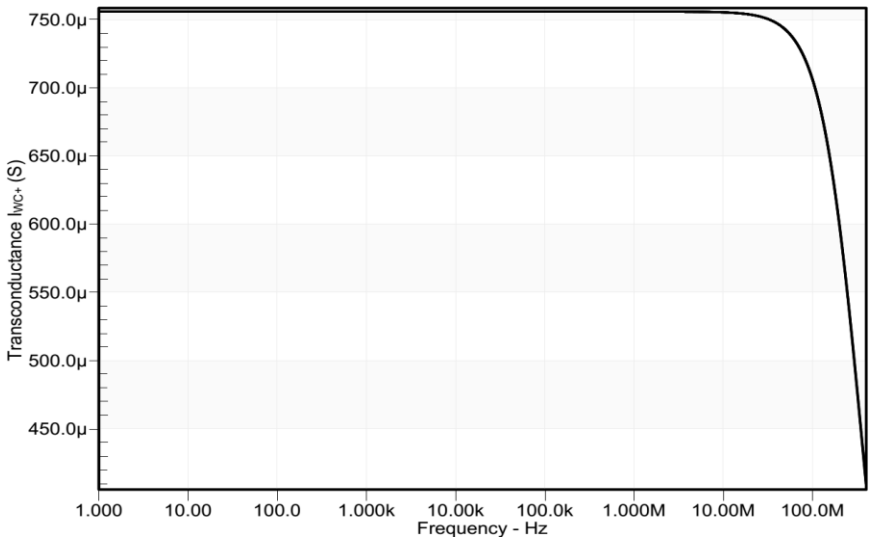


Figure 10: AC analysis of the OTA

The resistance for different terminals of the VD-DXCC are found by following the procedure given in appendix B. The resistances are found to be $R_{XP} = R_{XN} = 367\Omega$, $R_{ZP+}, = R_{ZN+}$=209.28 KΩ and $R_{WC+} = R_{WC-}$=138.14 kΩ.

4.3 Time Domain Analysis

The transient analysis results as presented in Figures 11 and 12 reveal that the voltage transfer and current transfer stages introduce negligible phase error and amplitude loss during signal transfer.

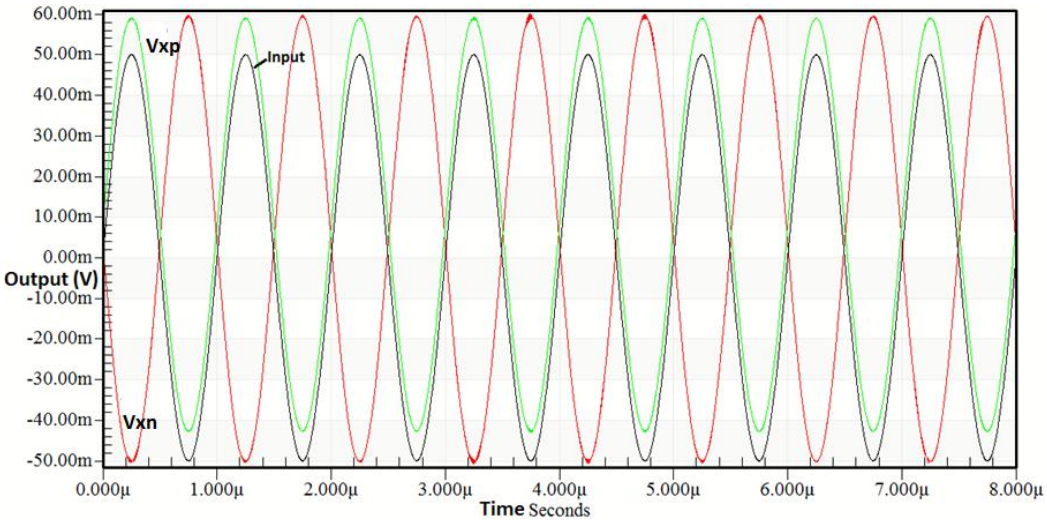


Figure 11: Time domain analysis of the voltage follower

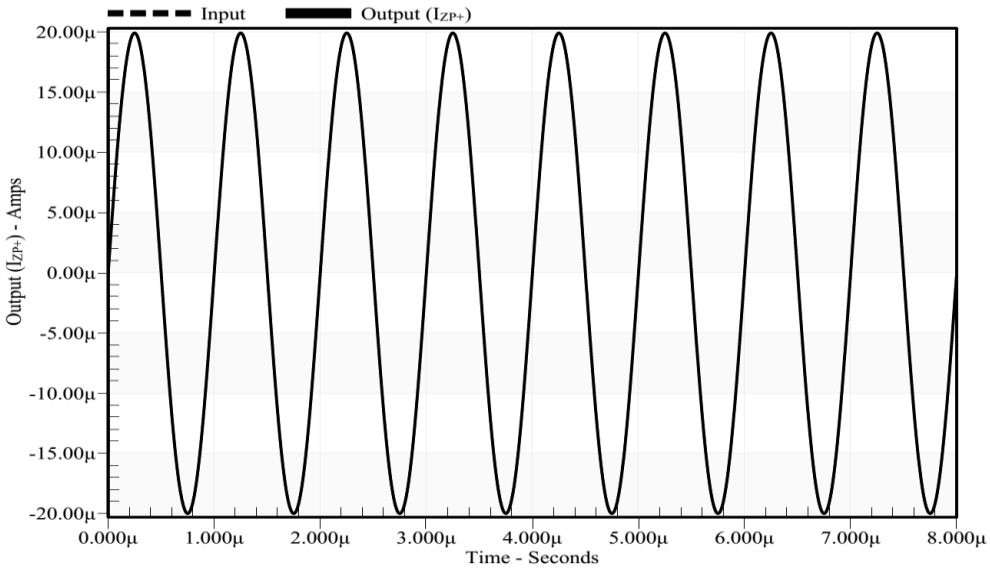


Figure 12: Time domain analysis of the current follower

V. CONCLUSION

In this study a low voltage low power (LVLP) VD-DXCC is designed using the floating gate technology. The LVLP VD-DXCC is a very versatile active block. It can be used in the design of analog filters, oscillators and active inductors. The VD-DXCC is design in 0.18µm bulk CMOS technology. The design is validated using Spice software. The VD-DXCC is designed for a supply of ±0.9V and AC, DC and transient analysis are done to validate the signal processing capability of the design.

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