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RKTG Pair Based Current Controlled Oscillator and Its Applications

Dr. Aram Singh and Rohitash Singh
Assistant Professor, Dayanand Vedic College Orai Jalaun UP
Associate Professor, Hindu college Moradabad UP

Abstract: -*In this research paper, we will present the design of a new current controlled oscillator (ICO). The current controlled of this IC0 is in order of nano or micro-Ampere range and the sensitivity of the frequency of its output voltage to the current control is about 100 kHz per uA. The circuit can run with a low supply voltage, e.g. VDD< 1 V when it is implemented with a 45-nm CMOS technology. It does not require bias current, soit has very low power dissipation. The circuit can be easily applied using a standard digital CMOS technology. Some applications of the suggested ICO, particularly those for A/D conversion, are also explained in above research paper.The work presented in this paper is about the design of current-controlled oscillators (ICO). Two ICOs are proposed. Aiming at reducing the duration of the short-circuit currents caused by slowly-changing voltages in the circuits, signal conversion blocks are introduced to generate sharp pulses. In this way, the power efficiency of the circuits is improved, which leads to an extensive performance improvement of the circuits. Both ICOs can operate over a frequency range from 100 KHz to 100 MHz. The quality of the output waveforms before buffers is good and over the entire frequency range the rise/fall time is consistently short. The power dissipation of the ICOs is very low, the same as that of a 5-stage current-starving ring oscillator. Moreover, the scheme of the ICOs allows an easy adjustment of the duty cycle of the output pulse signals. A simple digital control structure of the duty cycle has also been proposed*

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I. INTRODUCTION: -

Controlled oscillators, are useful circuits with particular use in telecommunications. Controlled oscillators are an integral part of phase-locked loop circuits. Clock or timing recovery circuits are necessary for data communications and storage systems. PLL circuits can also be applicable for FM modulation and demodulation. controlled oscillators have been used barely in sensor telemetry. Depending on the implementation, two performance parameters are overcritically important: low oscillator jitter is most important in clock recovery, whereas control linearity is of larger interest in FM modulation. The highest possible maximum oscillator frequency is often needed. In a relaxation oscillator both the maximum speed and the control linearity are linked to the total switching and comparison speed. Control linearity may be refined using negative feedback techniques [11] or compensation [2]. However, such type of schemes not only add complexity but also may affect the dynamic capacities of the oscillator. moreover, because the maximum oscillation frequency is ultimately examined by the comparison and switching delay, it is dominant that this delay be minimized. Jitter, or variable in oscillator period, has its origins in circuit noise. It has been shown that jitter is decreased by maximizing the capacitor voltage waveform amplitude [3], [4]. The amplitude can be increased by increasing the rail voltage, but this is usually neither requirable nor practical. In fact, to be compatible with currentprocesses, circuits use lower, not higher, voltages. Efforts to minimize jitter thus must concentrate on minimizing circuit noise, and maximizing the capacitor voltage amplitude for a given power supply voltage

Bipolar controlled relaxation oscillators are generally based on the emitter-coupled multivibrator. These circuits provide high speed and excellent temperature stability [5]. However, the high-power consumption of these circuits renders them inappropriate for some applications. moreover, MOS or CMOS compatibility is needed in many mixed-signal integrated systems.

Current-controlled oscillators are the main important building blocks in the design of electronic signal generation, processing or data-conversion circuits. Many of the existing ICO's are based on multi-vibrators or ring oscillators, in which multiple stages of delay elements are added. Logic gates and operational amplifiers are often applicable as such delay elements. In the former, the current available to charge or discharge a capacitance of each of the gates is adjusted in order to change the frequency of oscillation [11]. In the latter, the control current is used to adjust the circuit bias so that the gain of the OpAmps can he modified in order to adjust the frequency [Z] - [5]. In either case, a current variation of several nano-Amperes may not be large enough to result in a significant change of the frequency.

In this paper, we suggests the design of a current-controlled oscillator that is able to operate with a control current in order of nA or uA range. Some of the applications of the proposed circuit are also considered. Various MOS- or CMOS-controlled oscillator architectures have been proposed. For example, a monolithic controlled sinusoidal oscillator has been reported [6], and a number of high-speed CMOS-controlled ring oscillators (10-100 KHz) have been described [7], [8]. However, such circuits usually exhibit poor control linearity and are sensitive to device parameter variations.

The advantages of using grounded capacitors in relaxation oscillators have been stated in [9]. A very high-speed controlled NMOS relaxation oscillator, implemented in a 120um NMOS process, was described by Banu [l0]. This sub micrometer circuit implemented grounded timing capacitors using only parasitic and used simple digital latches, not precise analog comparators and a latch, to control charging. In this way, speeds of several hundred megahertz were achieved, but at the expense of capacitor switching voltage inaccuracy, and inconsistency. A general-purpose current-controlled relaxation oscillator is described in this paper [11]. The circuit allows relatively large capacitor voltage waveforms and so minimizes jitter. However, it is also compatible with present and future low-voltage fine-geometry CMOS processes.Additionally, because the circuit has no special requirements for linear capacitors, it can be implemented on a standard digital CMOS process.

Circuit Analysis: -In the below circuit shown in Fig.1 , the change of the state of the latch is done by means of the pull-down NMOS transistor N3 or N4. The voltage for the pull-down operation, Va or Vb, is built up gradually by the charge accumulation with the input current Iin. The transistor N3 or N4 is turned on during most time of the built-up process until Vd is pulled down and Vc is set up. Thus, the short-circuit current from the latch for this pull-down operation contributes significantly to the power dissipation of the circuit. As shown in Figure I, the proposed current-controlled oscillator consists of a CMOS latch (Inv1 and Inv2), a PMOS switch pair (PI and P2), and two NMOS switch pairs (N1 and N2, N3 and N4). Voltages Vc and Vd are, respectively, theorem and set signals of the latch, and Va and Vb, are the complementary output voltages of the circuit.

As P1 and P2 are controlled by Vc and Vd only one of them is turned on. The control current i, is thus switched to charge the gate capacitor of the transistor N1 or N2, raising the respective voltage Va or Vb. Then, the rising voltage becomes high enough to set (or reset) the state of the latch.

After that the current Ic will be switched to charge the other gate capacitor. Therefore, Ic is switched alternatively to the two gate nodes of N1 and N2, Va, and Vb are raised to the high level alternatively, i.e. the latch is set, or reset, alternatively, and Vc and Vd, change their levels periodically. Meanwhile, Vc and Vd, are applied at the gates of the two transistors, N3and N4, respectively, so that Va and Vb are pulled down to 0 V alternatively.

Aiming at a high performance of ICO circuits, the prime objective of this work is to develop an ICO scheme of very low power dissipation, high gain, wide range and simple structure. The ICO in [10] is able to provide almost all of them but its power dissipation may not be optimal. In this research paper, a new scheme based on [10] is presented and two ICOs are proposed. Besides, a structure of ICO with easy duty cycle adjustment is also presented.

The following points in the circuit design should be noted: -

1. A differential PMOS switch pair, controlled by the output voltages of the circuit, is used to steer the control current Ic, alternatively to the two nodes Va, and Vb.
2. The cycle time, K of the pulse signals depends on the time required for Va or Vb to be changed from zero to the level high enough to toggle the state of the latch. If the circuit structure are fixed and the device parameters are given, the frequency of the IC0 will depend on the voltage rate dVa/dt = ic/Ca and dVb/dt = ic/Cb, where Ca and cb are the capacitances at node Va and Vb respectively. As all the switches can be minimum-sized transistors, Ca and Cb are usually small. A small current variation of the control current can make a significant change in the voltage variation rate. Thus, the frequency can be highly sensitive to the current variation. This feature also implies that the decrease of transistor feature size leads to a decrease in Ca and Cb i.e., an increase in the sensitivity of the ICO to the control current.
3. A very weak control current may result in a relatively long rise time of Va and Vb However, the rise or fall time of the output signals, Vc, and Vd, depends mainly on the current driving capacity of the inverters and the regenerative process of the latch. Thus, the quality of the output pulses of the ICO is not affected by the weak control current.
4. Six MOS switches are used to switch the control current and discharging currents. All these switches are controlled by the voltage signals generated in the circuit. The circuit is, in fact, a switched-current circuit operating without any external control voltages.

II. SIMULATION RESULTS: -

The IC0 (Figure I) has been simulated using the transistor models of a 45nm technology. All the transistors of this IC0 are minimum-sized. The waveforms of the signals, when the control current Ic = 1u A and the supply voltage VDC = 10 V, are shown in Figure 3.

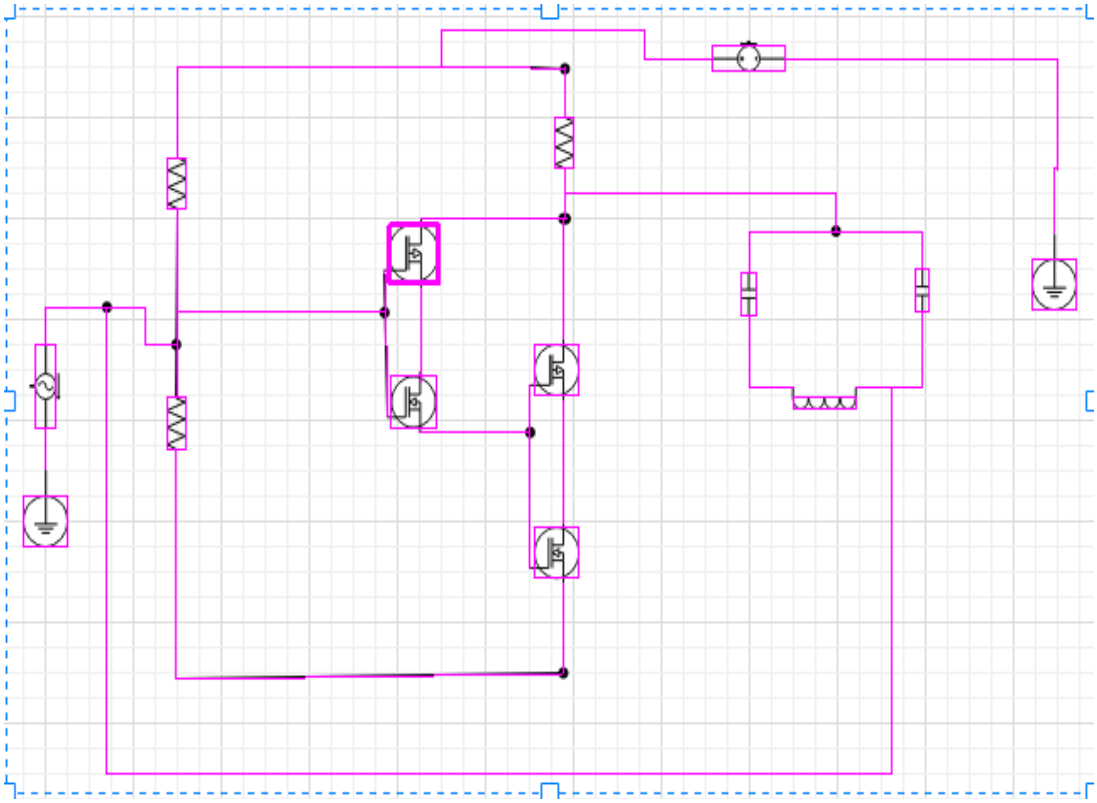

Fig- 1 RkTG pair based current controlled oscillator

Figure 4 illustrates the frequency-versus-current characteristics of the circuit. Due to the limitation of appropriate use of the transistor models, the minimal value of Ic is chosen as 1u A in the simulation. However, we can be sure that. in practice, the control current can be much lower. The sensitivity of the IC0 is about 10 MHz/nA. The power dissipation of the circuit depends on the frequency of the output voltage and it is 10 uW when the output frequency is about 100 KHz.

Proposed RKTG pair oscillator circuit provides good transient response with stop time 100 ms. Simulated result is shown in fig.3. So the proposed oscillator circuit is used with proper choice of component to provide the wide range frequencies. This circuit works at 10 microwatt power dissipation.

III. APPLICATIONS:-

ICO circuits, in general, can he used in signal processing and communication systems for example, in frequency modulation or signal generation. It can also be an important part in a PLL circuit. However, the proposed IC0 is particularly useful for optical signal sensing and processing. An incident light can he converted linearly into a current signal and then this current can be processed by the circuits involving the IC0 and other processing units. In this process, two features of the proposed IC0 need to he highlighted. First, the high sensitivity of the frequency of the proposed ICO to the input current makes the circuits capable of effectively responding to very weak currents converted from optical signals. Thus, the application of the IC0 can improve the circuit's capability of operating with weak optical signals. Second, the ICO converts a current signal into a voltage one that carries the information through the duration of its cycle, instead of its magnitude. The dynamic range of the circuit is, therefore, not limited by the supply voltage, thus making the circuit to have a large dynamic range as well as a high sensitivity. Since the ICO converts an analog current signal to a voltage pulse signal, it is obviously to be used for an A/D conversion. Figure 2 shows such an example. The photocurrent ia converted from the incident signal is fed to the ICO. The number of the pulses of the output of the IC0 is then counted during a period of T that is related to the weakest input signal. At the end of the period, the counter will output a n-bit digital signal converted from the input current of the ICO

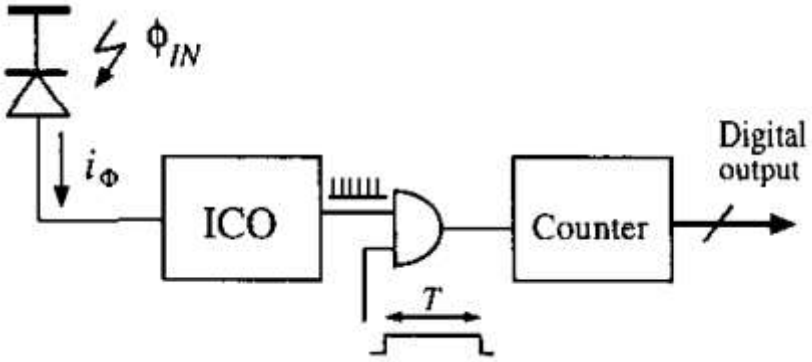

Fig-2 Diagram of a circuit performing optical-to electrical conversion and AID conversion.

As the IC0 outputs a voltage pulse signal, the information carried by its analog input can be processed digitally. The circuit shown in Figure 3 is such an example. This circuit has two optical incident signals, and its operation is controlled by a clock signal clk. The IC0 can also be used for data conversions along with other types of computations. An example is shown in Figure 4. In this circuit. the pulse width of the output

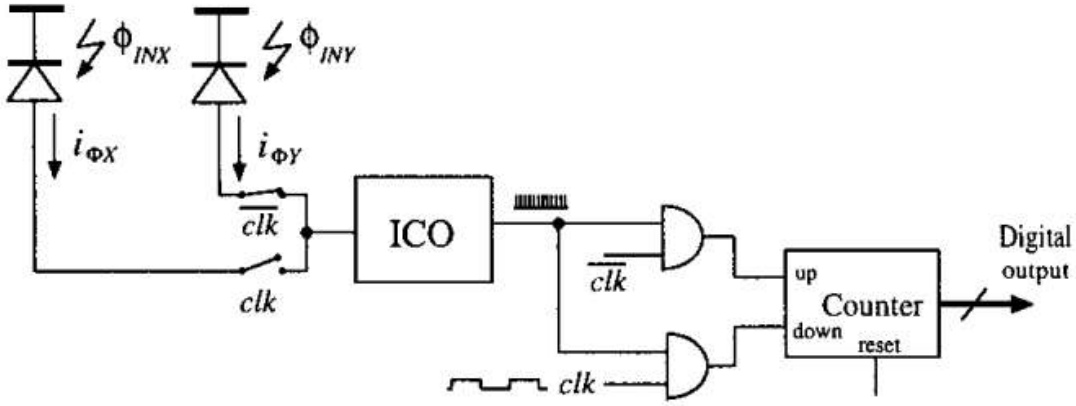

Fig.3 Diagram of a circuit performing optical-to-electrical conversion. subtraction and AID conversion.

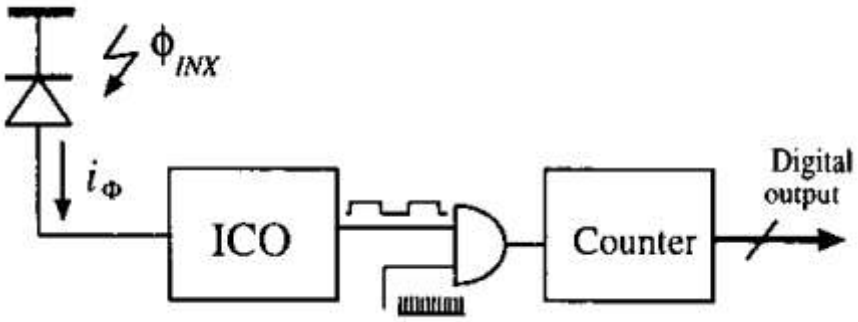

Fig.4 Diagram of a circuit of which the digital output is inversely proportional to the incident intensity

IV. CONCLUSION:-

A current-controlled oscillator suitable for fine-geometry CMOS has been described. The oscillator was implemented in an analog process; however, because the circuit has no special capacitor requirements, it is equally suited to a digital process. To minimize jitter, the oscillator structure permits large capacitor voltage waveform amplitudes. The use of a high-speed double-differential latching comparator allows fast operation with high control linearity.The proposed IC0 is a CMOS latch-based switched-current circuit. Compared to most of the existing IC0 circuits, the new circuit has a simpler structure, higher sensitivity, better ability to operate in nano-Ampere range or below with a very low supply voltage, and lower power dissipation. Moreover, the circuit does not need external control/bias signals and can be easily implemented using a standard digital CMOS technology. From above discussion it is concluded that the RKTG pair circuit played an important role with proper choice of the circuit element. The circuit work as an oscillator circuit for higher frequency with five

microwatt power dissipation which can be useful for 5th generation mobile communication system in coming future and various communication system. Thus solving real challenges in the future we have designed and simulated RKTG pair circuit with the addition of few other circuit elements to yield high frequency high speed with low power loss oscillator with wide band of frequencies upto 100KHz which may be extended upto 100 MHz or more for which further work is going on. It is seen that such circuit are useful for functional integration rather scale integration.

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