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Field Programmable Analog Array based on DOCCCII and its Application

[1]Deepak Kumar Yadav, [1]Umesh Singh, [1]Sanjay Chauhan
[1]*Department of Electronics, Institute of Engineering and Technology, Dr. Ram Manohar LohiaAvadh University, Ayodhya, India*
Corresponding Author:deepakyadav85@gmail.com

Abstract
Field programmable analog arrays (FPAAs) provide a method for rapidly prototyping analog systems. Analog systems like filters and amplifiers are needed in every digital IC. Although digital signal processing (DSP) algorithms are more developed and can handle complex processing tasks then analog signal processing (ASP). ASP has its advantages in terms of higher bandwidth, low power dissipation and less area consumed. In this paper we have designed a Dual output current controlled current conveyor (DOCCCII) in 0.18µm CMOS technology using PTM (High Performance 16nm Metal Gate / High-K / Strained-Si parameter) and discussed its ac characteristic. A configurable analog block (CAB) is proposed for FPAA implementation which mainly consists of the DOCCCII readily configurable to realize several analog applications like integrators, 1st and 2nd order filters, oscillators, and amplifiers etc.

Keywords: *Analog circuits, Current mode, Current conveyor, Signal processing*

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I. INTRODUCTION

Digital systems are dominating the market for VLSI applications; analog design still maintains its position by interfacing digital systems with the real world. Every digital IC has an analog circuitry for preprocessing of signals and interfacing. There are certain applications that can be realized only in analog domain like filters, amplifiers, oscillators, etc. Designing analog circuits is multidimensional problem where a number of tradeoffs need to be considered. FPAA is needed which facilitates rapid prototyping of analog circuits. In many imminent literatures FPAA based on current mode devices including current feedback operational amplifier (CFOA), second generation current conveyor (CCII) and its variants has been proposed [1-20]. This work can be considered significant on the basis of various design matrices like high frequency, low power and low voltage [3-5] etc. Among different current mode circuits, current conveyor (CC) attains greater importance due to its versatility in applications in low voltage low power VLSI. A CC offers both low impedance input and high impedance input nodes simultaneously along with a voltage virtual short amongthe various input nodes like a conventional OPAMP [9, 10]. It exhibits improved slew rate, very high gain bandwidth product, larger dynamic range, greater linearity, small chip area, low power consumption [11-16] and Current controlled current conveyor (CCC) is another version, which exhibits a considerable resistance at the low impedance or current input (node *X*).. A practical CC is deviation from ideal behavior, known as non-idealities [17,18]. Some of these non-idealities play important roles, e.g. the parasitic resistance at the low impedance node (R_X) leads to define a CCC. Likewise, other non-idealities also sometimes exhibit similar favorable effects [17]. Current negation and current duplication is very easy to obtain in case of a CCC, leading to DOCCC, MOCCC etc. 2nd generation is generally preferred, therefore CCCII, DOCCCII etc. are readily seen in literature. Here in this paper, we have designedone configurable analog blocks (CAB) using the translineardual output current controlled current conveyor (DOCCCII), realized in 180nm bulk CMOS Technology using the PTM [21] CMOS model parameters.

II. DUAL OUTPUT CURRENT CONTROLLED CURRENT CONVEYOR (DOCCCII)

The dual output current controlled current conveyor (DOCCCII) has parasitic resistance R_X at the current input node and is tunable by the biasing current I_B [15,17]. A DOCCCII provides a current signal and its quadrature signal simultaneously. The equivalent circuit symbol and the principal equation of DOCCCII are given in Figure 1 and equation 1 respectively.

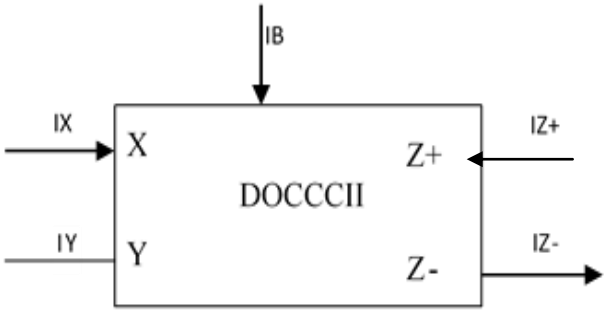


Figure 1: Block diagram of DOCCCII

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} R_X & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} (1)$$

The CMOS implementation of a class AB DOCCCII is presented in Figure 2. The circuit consists of a translinear loop consisting of transistors M1 – M4. Two MOS current mirrors (M5 – M6 and M7 – M8) are used to bias the translinear loop with bias current I_B, the input cell presents a high input impedance at input port *Y* and a low input impedance at input port *X*. This cell acts as voltage follower. The current at node *X* is copied to output nodes *Z*+ and *Z*–. Currents *Id18* and *Id14*are cross-coupled through transistors M14, M15, M18 and M19 to generate negative current at *Z*- node. Details are shown in circuit below.

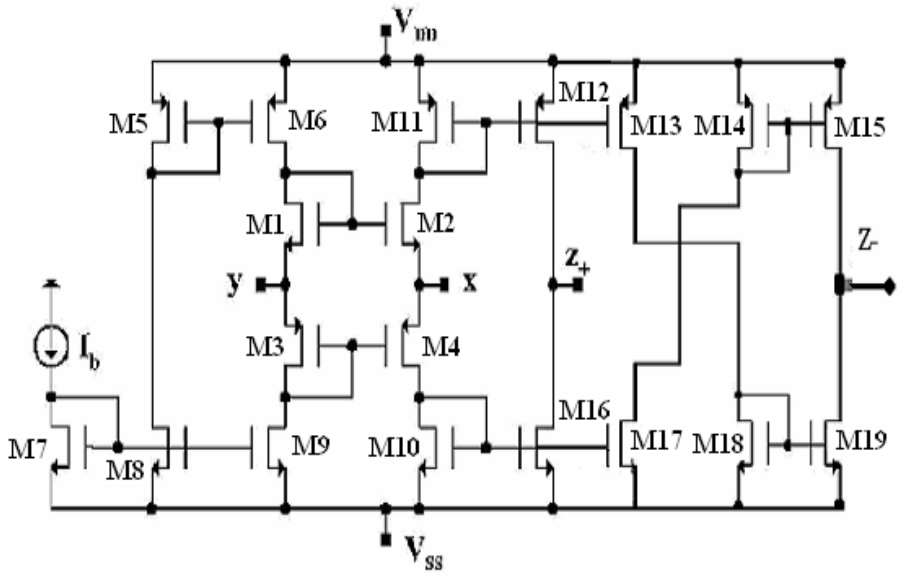


Figure 2:CMOS Implementation of DOCCCII

III. DOCCCII BASED CAB

A configurable analog block (CAB) is a block which can realize an application configurable in user domain. In the present work a pair of CAB's is proposed which can accommodate a larger application spectrum, particularly, the quadratic or biquadratic applications, including various analog filters and sinusoidal oscillators. The presented CAB contains aDOCCCII, a conjoin of capacitor and resistor at node *Y*, a capacitor at node *Z*- and X and switches *S1 – S7*. ThisCABis presented in Figure 3. In order to include the required capacitors and resistor respective NMOS switches associated with them are closed to configure the CAB for a given application. A number of these CABs can be used to construct FPAA and connected together through the switching matrix to realize variety of different applications. The switch is no more ideal but is a jargon of large number of non-idealities like offset voltages and currents and various parasitic resistances, inductance and a large number of capacitances. Some of them are important in consideration with FPAA scheme as their effects are dominant. Therefore, consideration is that their effects do not alter the circuit performance altogether. Here in this work, we try to swamp the switch dominance over the application. For this purpose, an estimate is made

for the total effect of various capacitances connected to a node and is assumed as a lumped model of the total capacitance at the node (e.g., C_{GTOTAL}), also suggested byHSPICE. Besides this, channel resistance is also considered in our model. This model is affected by adjusting the external capacitance values and the switch aspect.

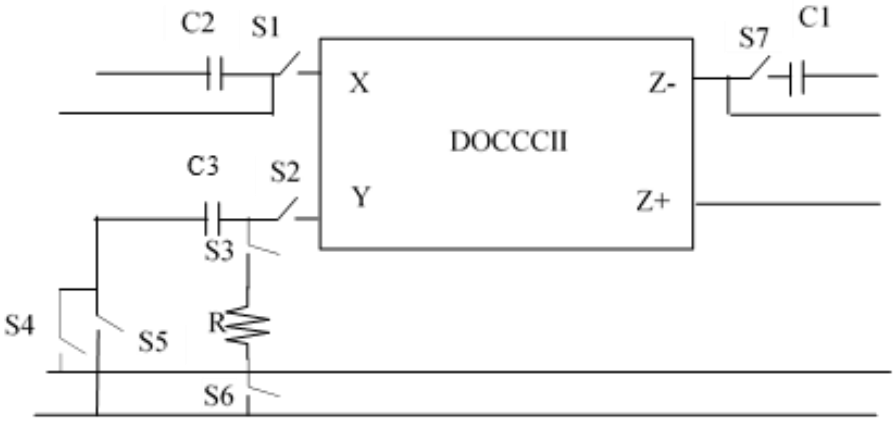
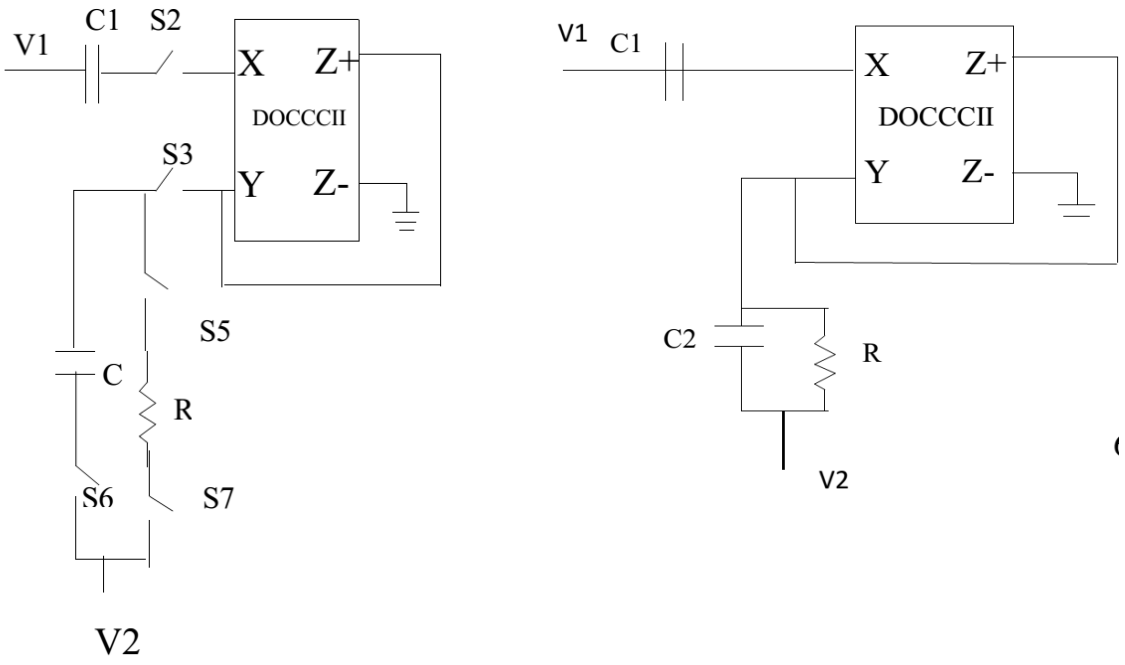


Figure 3:Configurable analog blocks

IV. RESULT AND DISCUSSION

The performance of the DOCCCII and the CAB based on it is verified by performing H-spice simulations using 0.18µm CMOS technology. The working of the proposed CABmodel is demonstrated by running an application with the original circuit and then the same application is realized by using the proposed CAB. The applications realized include second-order band-pass and notch pass filter from the already published work. In figure 4(a) a filter structure given in [22] is realized using the designed CAB.To include the required components on to various nodes their respective switches are closed namely (S2,S3,S5,S6,S7). The figure shows the original circuit of [22] without switches. To study the performance of the CAB based design both the original circuit and the circuit realized using the CAB are simulated. The figure 5 and figure 6 confirms the performance of the CAB based circuit is nearly same as the original circuit.



(a) (b)

Figure 4(a) and 4(b): Realization of filter using CAB and without CAB

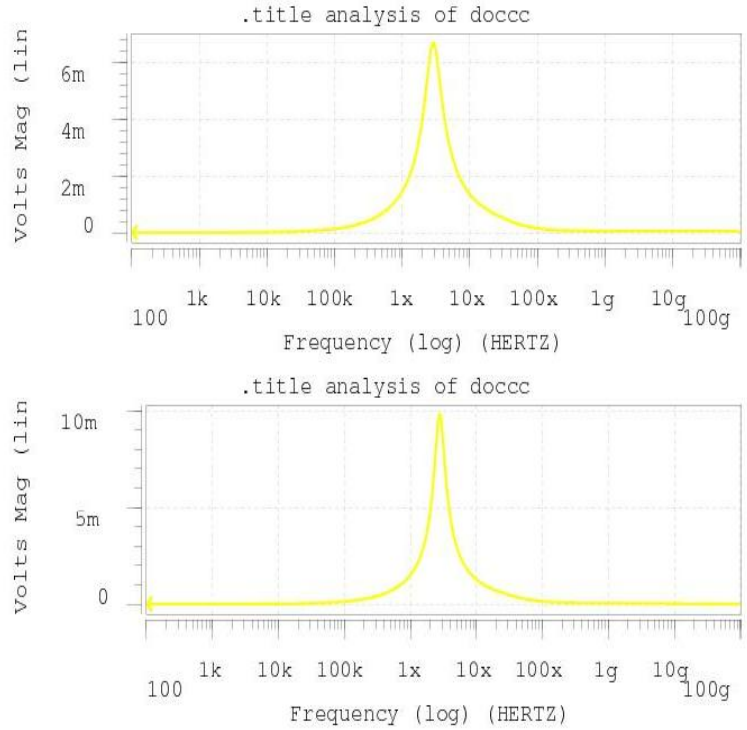


Figure 5: Simulation response of notch pass filter using figure 4(a) and figure 4(b)

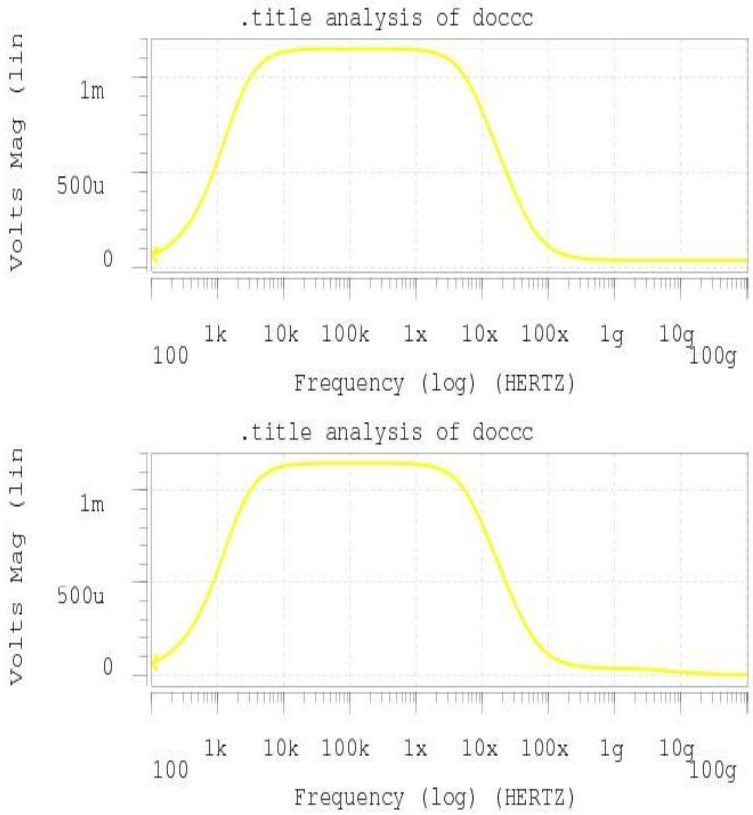


Figure 6: Simulation response of band pass filter using figure 4(a) and figure 4(b)

V. CONCLUSION

A new design for configurable analog block based on DOCCCII for high frequency applications is proposed. Using this CAB together with programmable interconnect FPAA can be constructed which will efficiently realize a number of 2nd order filter topologies, oscillators and amplifiers.

REFERENCES

[1]. X.Quan,S.Embabi,andE.Sanchez-Sinencio, "A current-mode based field programmable analog array architecture for signal processing applications,"inproc.IEEE Custom Integr. Circuits Conf.,May 1998,pp.277-280.

[2]. G.Kapur, S.Mittal, C.M.Markan, V.P.Pyara, "To develop a design methodology for a Analog Field Programmable CMOS Current Conveyor", proceedings of IEEE student conference SCES 2012, MNNIT, Allahabad, 16th -18th March, 2012.

[3]. S. H. K. Embabi, X. Quan, N. Oki, A. MANJREKAR AND E. Sa'nchez-Sinencio, A Cuurent -Mode Based Field Programmable Analog Array for Signal Processing Applications, Analog Integrated Circuits and Signal Processing,Vol17,Issue 1-2,pp 125-142 .1998

[4]. Vincent C.Gaudet. Glenn Gulak " CMOS Implementation of a Current Conveyor-Based Field-Programmable Analog Array", 1058-6393/98 IEEE.

[5]. Soliman Mahmoud,Eman Soliman, "Novel CCII-based Field Programmable Analog Array and its Application to a Sixth- Order Butterworth LPF. Journal of Circuits, Systems and Computers" Journal of Circuits,Systems and Computers, volume20,Issue 08,December 2011.

[6]. S. Sedra, G. W. Roberts, and F. Gohh, "The current conveyor: History, progress and new results," Processing. Institute. Elect. Eng. Part G, vol. 137, no. 2, pp. 78–87, Apr. 1990.

[7]. R. Senani, "Novel circuit implementation of current conveyors using an OA and an OTA," Electron. Lett. , vol. 16, no. 1, pp. 2–3, January 1980.

[8]. B. Wilson, "Recent developments in current conveyors and current mode circuits," IEE Processing, Pt. G, vol. 137, pp. 63-77, April 1990.

[9]. C. Toumazou, A. Payne, D. Haigh. "Analogue IC design: The current mode approach", Peter Peregrinus 1990.

[10]. Giuseppe Ferri and Nicola .C.Guerrinni, "Low voltage low power CMOS current conveyors", Print ©2003 Kluwer academic publishers, Dordrecht

[11]. B. Wilson. "Constant bandwidth amplification using current conveyors". International Journal of Electronics, no. 65, pp. 893-898, 1988.

[12]. Zia Abbas, Giuseppe Scotti and Mauro Olivieri, "Current controlled current conveyor (CCCII) and application using 65nm technology", World Academy of Science, Engineering and Technology 55, 2011

[13]. C.H. Lee, J. Cornish, K. McClellan, J. Choma Jr., "Current-Mode Approach for Wide-Gain Bandwidth Product Architecture", IEEE Trans. Cir. Sys. II, Vol. 45, May 1998.

[14]. L.N. Alves, R.L. Aguiar, "A Differential Current-Conveyor Based Buffer for High-Bandwidth Low-Signal Applications", ICECS99, Paphos, Cyprus, Sep.

[15]. A.Fabre, O. Saaid, F. Wiest, and C. Baucheron, High frequency applications based on a new current controlled conveyor, IEEE Transactions. Circuits System-I, vol. 43,no. 2, pp. 82-90, 1996F. Yuan, CMOS Current-Mode Circuits for DATA Communications, Springer Verlag, 2007.

[16]. M.Y.Yasin, Bal Gopal "High Frequency Oscillator Design Using a Single 45 nm CMOS Current Controlled Current Conveyor (CCCII+) with Minimum Passive Components" Circuits and Systems,2011,2,53-59, doi:10.4236/cs.2011.22009

[17]. PipatPrommee,Montrisondunyakanok, " CMOS based current controlled DDCC and its applications to capacitance multiplier and universal filter" Int.J.Commun.(AEU) 65 pp.1-8, 2011.

[18]. M.Y.YASIN. "A Novel bipolar XOR/XNOR realization using translinear type 2nd generation current controlled current conveyor designed in 45 nm CMOS technology",Actaelectrotechnicha,vol.54, no.1, pp. 3-6, 2013;

[19]. Firdaus Majeed. "Low voltage low power redesign of CCCII in 45 nm CMOS technology and its analog and digital applications" M.Tech thesis , May 2011,selected 3rd by IAS-IEEE;IEEE industry applications magazine,vol.17, no.6,pp.74, ISSN 1077-2618,Nov-Dec 2011

[20]. Firdaus Majeed, M.Y.Yasin, "A novel voltage comparator and its application-A new simple configuration based on 45 nm 2nd generation CMOS current controlled current conveyor", Mediamira Science publisher,vol.53, no.2,2012.

[21]. Predictive Technology Model, 2006 http://ptm.asu.edu.

[22]. Jai Prakash,PradepKumar,"Voltage Mode Second Order BiquadraticFilters Using Single CCCII" international Journal of Electronics Engineering, vol. 3,pp. 257-260, 2011.