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Lossy and Lossless Grounded Inductor Simulators with Electronic Tunability

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Abstract
In this paper two new designs of lossless grounded inductor simulators (GIS) are proposed. The designs employ a highly versatile active element the dual X current conveyor differential input transconductance amplifier (DXCCDITA). The inductor simulators require three passive components, two grounded resistors and one capacitor. The realised inductance can be tuned electronically. There is no need of passive component matching for realizing the inductance. The non-ideal analysis is carried out to study the effect of process and component spread on the performance of the designed GIS. The simulations are conducted using 0.35 µm CMOS technology at a supply voltage of ±1.5 V. LTspice software is used for the analysis.
Keywords: *Analog circuits, Current mode, Current conveyor, Signal processing*

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I. INTRODUCTION

Inductors and capacitors are indispensable components in analog circuits [1]. The major limitations curtailing the use of the synthetic inductors are their bulky nature, high cost, requirement of large silicon area and lack of electronic tunability [1-2]. The floating capacitors with large values are also difficult to design and fabricate. Moreover, the current fabrication technology supports monolithic inductors of around 1nH and limited quality factors [1-2]. This led to the research in the active simulation of inductors and capacitors. The generalized active immittance simulators finds applications in LC oscillators, for parasitic cancellation, impedance matching, active filters, phase shifters and resonators etc. [1-6]. The immittance simulation can be divided into two categories grounded immittance and floating immittance simulation. The actively simulated immittance include inductors, capacitor multipliers and frequency dependent negative resistors.

The inductor simulation finds multitude of applications especially in higher order filter design. A popular method of higher order filter synthesis is LRC ladder filter simulation. It also a well-established fact that a ladder filter has minimum components sensitivity. The major limitation that arises in ladder filter simulation is the requirement of high valued one or more grounded or floating inductors which render it incompatible with today's low voltage and miniature size systems. In order to judiciously use each micron of chip area researchers utilize inductor simulation techniques in which an active element along with RC components emulate the behavior of a passive inductor. This approach provides many advantages to elaborate a few (i) the chip area required is reduced (ii) large value inductors with acceptable quality factors can be synthesized (iii) by employing modern active blocks like current conveyors on chip tunable inductors can be developed (iv) floating inductors can also be easily realized. Another important simulation is that of capacitor multiplier. In some filter applications large, valued capacitors are required which are difficult to fabricate owing to large chip area. Moreover, present day's deep submicron technology does not support large valued integrated capacitors. To overcome this scenario, active simulation of capacitors where active device along with small values RC network emulated the behavior of a large passive capacitor. A small value capacitor along with resistors and active blocks give large value active capacitors, hence the capacitor multipliers.

The inductor simulators can be categorized based on number of active blocks used, number of passive elements employed and whether they emulate lossy or loss less inductance. The simulators presented in [1, 11-13, 15, 16, 17, 21-23] use single active block but require passive components more than three and also passive components matching to realize inductance. The designs proposed in [5, 10, 12, 14-17, 19, 21-24] use one or more floating capacitors and/or resistors for implementing inductance. Although floating capacitor can be easily fabricated in the modern technology. The use of floating capacitor is not desirable for integrated circuit implementation as it requires die area and effects noise performance. The designs proposed by [4, 12, 13, 23] employ two or more active blocks and excessive passive elements resulting in more chip area and parasitic effects. The designs proposed in [1, 4, 5, 11-24, 29, 30] did not provide inbuilt tunability of the inductance. The designs in [10, 28] have inbuilt tunability to tune the simulated inductance which is very advantageous. A detailed comparison of the exemplary inductance topologies available in the literature is done. The literature survey reveals that the drawbacks of the majority of the presented inductor simulators are (i) no provision for on chip tunability (ii) use of more than one active element (iii) use of floating capacitor (iv) excessive use of passive elements (v) passive components matching requirement.

II. Dual X Current Conveyor Differential Input Transconductance Amplifier (DXCCDITA)

The Dual X current conveyor differential input transconductance amplifier (DXCCDITA) [31] is a very flexible active element that has features of current conveyor (CCII), inverting current conveyor (ICCII) and operational transconductance amplifier (OTA) in a single integrated package. The OTA provides inbuilt tunability to the active element. The block of DXCCDITA is given in Fig.1 and the current-voltage relations are presented in Equations (1-6).

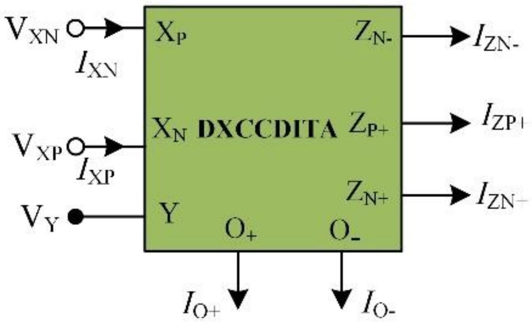

Figure 1. Block Diagram of DXCCDITA

$$I_{XP} = I_{ZP+} = -I_{ZP-} \quad (1)$$

$$I_{XN} = I_{ZN+} = -I_{ZN-} \quad (2)$$

$$V_Y = V_{XP} = -V_{XN} \quad (3)$$

$$I_{O+} = -I_{0-} = g_m(V_{ZP+} - V_{ZN+}) \quad (4)$$

The expression for transconductance (g_m) is given in Equation 5.

$$g_m = \sqrt{\mu_n C_{OX} \left(\frac{W}{L}\right)_{25,26} I_{Bias}} \quad (5)$$

where C_{OX} is the gate oxide capacitance, μ_n is the mobility of electrons in NMOS, g_m denotes the transconductance of OTA set via bias current I_B and $\frac{W}{L}$ is the aspect ratio of the transistors.

The CMOS implementation of the DXCCDITA is presented in Fig. 2. The f is low impedance current input node. The X_+, X_-, Z & Z_C terminals are high impedance current output nodes. The number of current output terminals (I_{ZC}, X_+, X_-) can be increased by simply adding two MOS transistors.

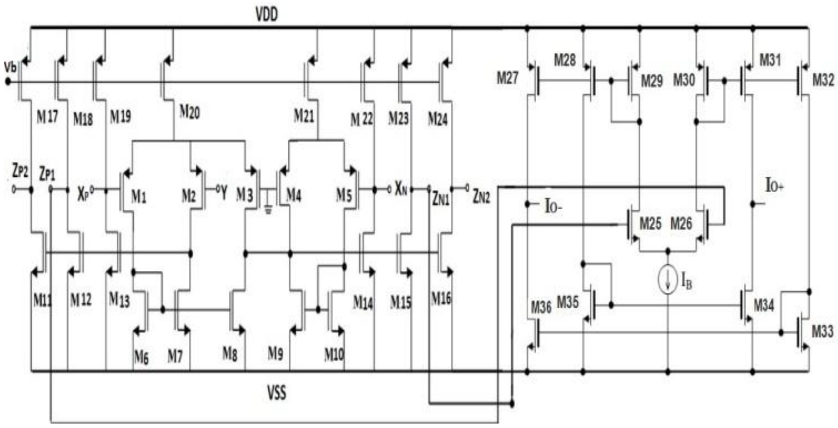

Figure 2: CMOS implementation of DXCCDITA

III. Non-Ideal Analysis of DXCCDITA

The proposed inductor simulators using a single DXCCDITA, and grounded passive elements are shown in Fig.3. The analysis of the circuits leads to the inductance values as presented in Equations (6-7). The proposed inductors have inbuilt tunability and requires minimum number of passive components. Additionally, there is passive components matching for realizing the inductance.

Inspection of Equations (6-7) reveals that the GIS-1 and GIS-2 realize pure inductance.

$$L_{eq} = \frac{V_{IN}}{I_{IN}} = \frac{\mathrm{SC_1R_1R_2}}{\mathrm{g_m(R_1+R_2)}} \tag{6}$$

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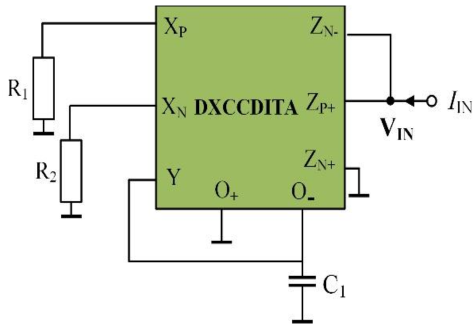
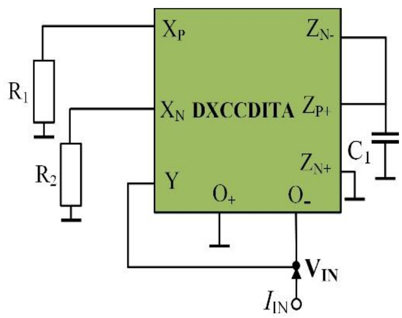


(a)



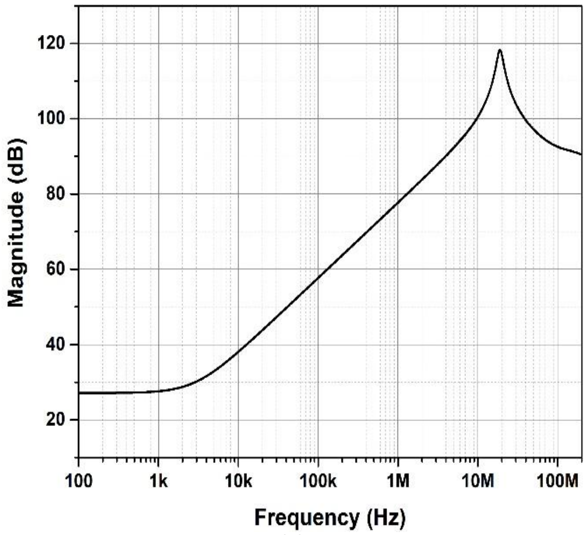
(b)

Figure3: Proposed Inductor Simulators (a) GIS-1 (b) GIS-2

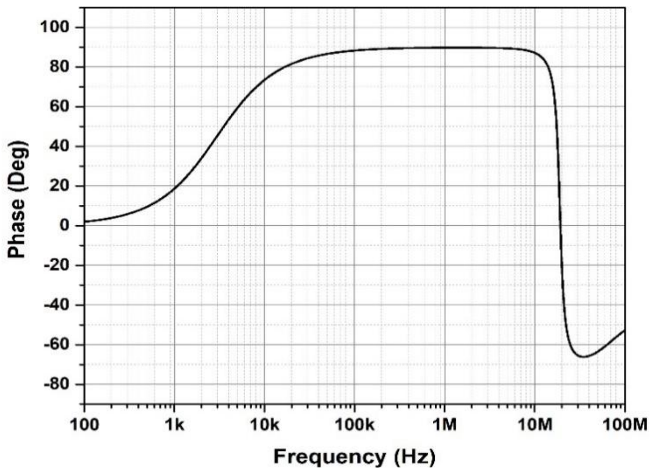
IV. RESULT AND DISCUSSION

To test the proposed inductor simulators the DXCCDITA is designed in CMOS 0.13µm TSMC technology. The simulations are carried out in LTspice software for validating the designs. The DXCCDITA is simulated at a supply voltage of ±1.5V. The bias current of the OTA was fixed at 50µA to set the transconductance (g_m)=0.1mS.

The GIS-1 is examined by designing for L=1.25mS by selecting $R_1 = R_2 = 5k\Omega$, $C_1 = 50pF$ and g_m=0.1mS. AC analysis is conducted to test the grounded inductor GIS-1. The gain and phase graphs as presented in Fig. 4 shows that the inductance behaviour is shown from 5kHz till 15MHz.



(a)



(b)

Figure4: The GIS-1 (a) gain and (b)phase response

To check the tunability of the realised inductance the bias current of the OTA was varied from 20µA to 60µA and the AC analysis is done as shown in Fig. 5. It can be deduced from the graph that the inductance can be tuned which is an advantage.

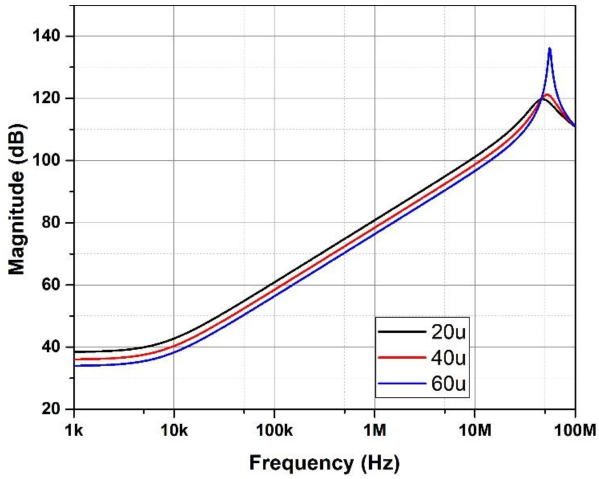
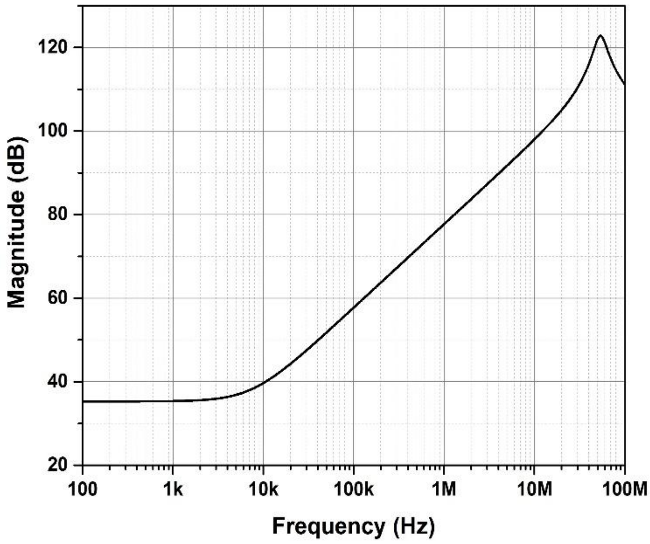
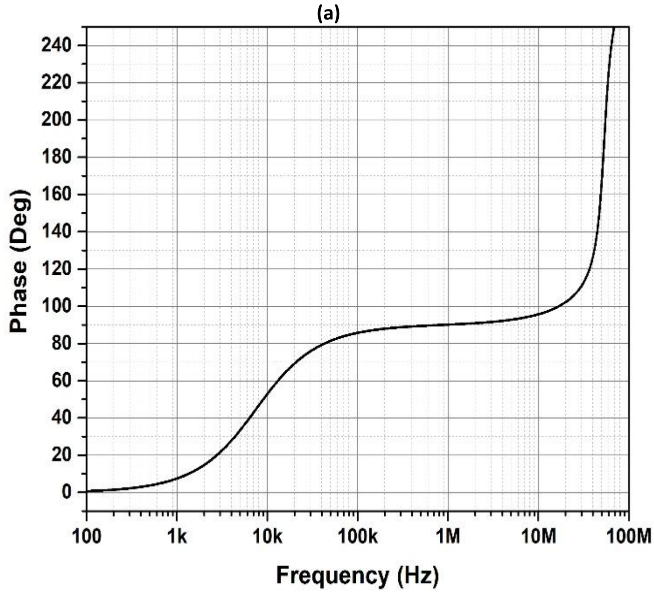


Figure5: The GIS-1 tunability analysis

Next the GIS-2 is analysed by designing for L=1.25mS by selecting $R_1 = R_2 = 5k\Omega$, $C_1 = 50pF$ and g_m=0.1mS. The AC analysis results presented in Fig. 6 confirms the working.



(a)



(b)

Figure6: The GIS-2 (a) gain and (b)phase response

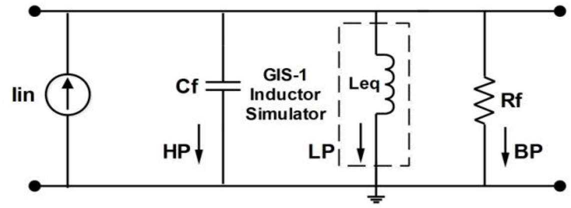


Figure7:The current mode filter topology

$$\omega_o = \frac{1}{\sqrt{L_{eq} C_1}} \tag{8}$$

To test the practical application of the proposed inductor simulators they are employed for the design of frequency filters which are an essential building block of any communication system. The Fig. 7 shows a passive current mode filter. The passive inductor in the filter is replaced by the active GIS-1 active inductor. The filter is designed for a frequency of 1.5MHz using the expression for frequency given in Equation 8. The passive components values are set to $R_f = 10k\Omega, C_f = 10pF$ and$L_{eq} = 1.25mH$. The bode plot given in Fig. 8of the filter confirms the practical applicability of the designed GIS-1.

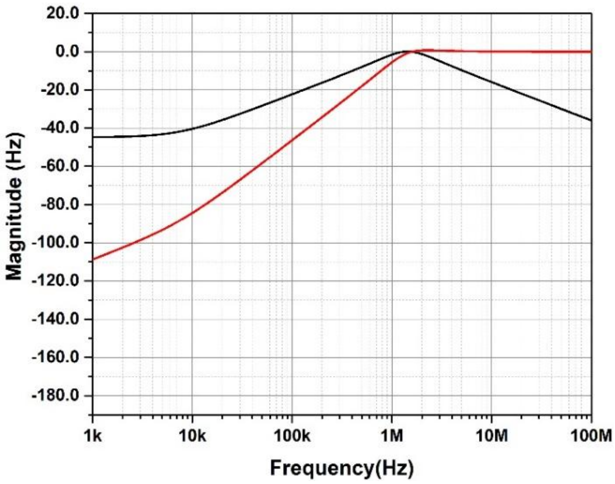


Figure8:Frequency response of Current mode filter

The GIS-2 is employed for the design of current mode HP filter. In the filter presented in Fig. 9 the passive inductor is replaced by active GIS-2. The filter is designed for a frequency of 500kHz by setting passive components values as $C_f = 100pF, R_f = 10k\Omega$ and$L_{eq} = 1mH$. The expression for frequency is given in Equation 9. The AC analysis results presented in Fig. 10 confirms the practical use of GIS-2.

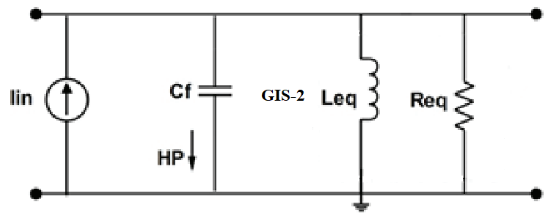


Figure9: The current mode HP filter topology

$$\omega_o = \frac{1}{\sqrt{L_{eq} C_f}} \tag{9}$$

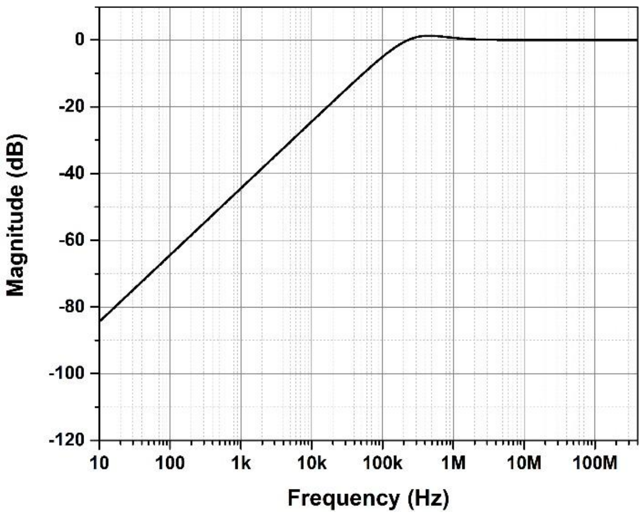


Figure10:Frequency response of Current mode HP filter

The time domain analysis of the HP filter is carried out to check the signal processing capability of the filter. A sinusoidal current signal of 80µVp-p is applied at the input and the output is examined. The plots in Fig. 11 show that the filter is working correctly.

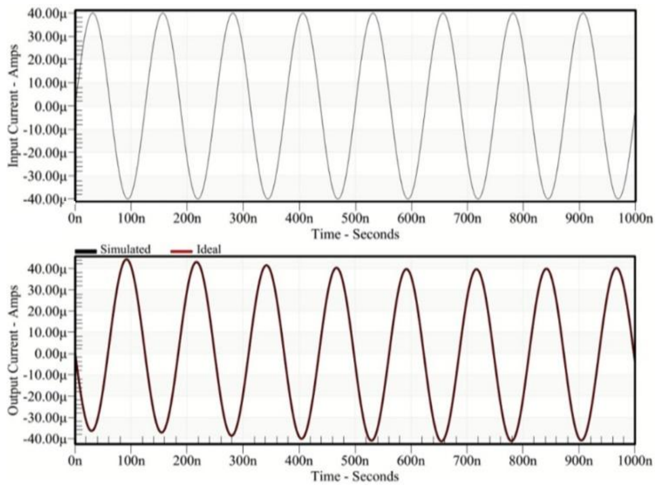


Figure11:Time domain analysis of the current mode HP filter

V. CONCLUSION

This paper presents two new designs of grounded lossless inductor simulators employing DXCCDITA. The proposed inductor simulators require only grounded passive components for realization and have electronic tuning capability. The proposed simulators are examined using mathematical analysis and the effect of non-ideal current and voltage gains on their performance is also examined. The inductor simulators are validated by using them to design many passive filter circuits. The LTspice software is used for the design and verification. The simulation results are found consistent with the theoretical predictions.

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